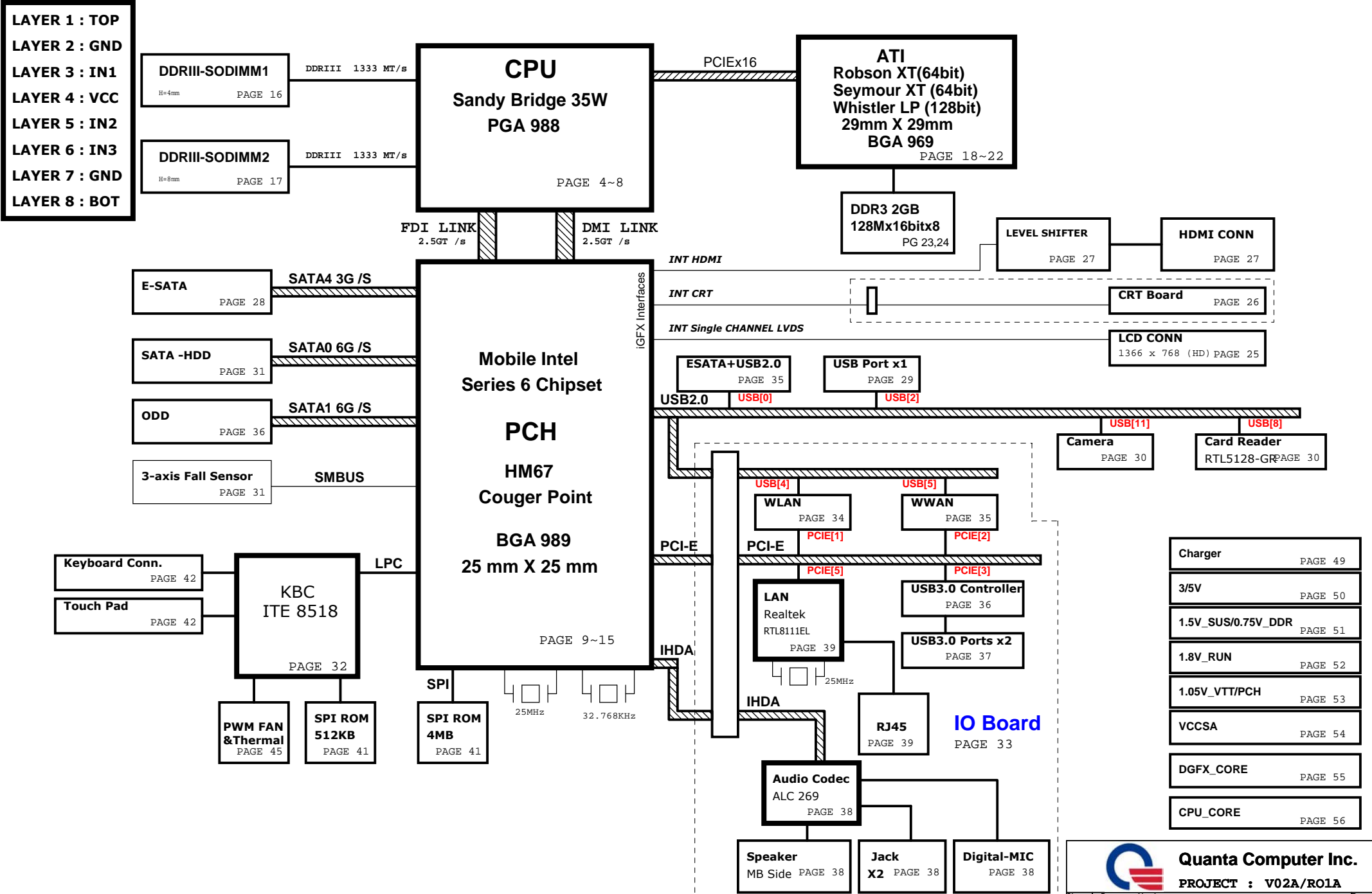


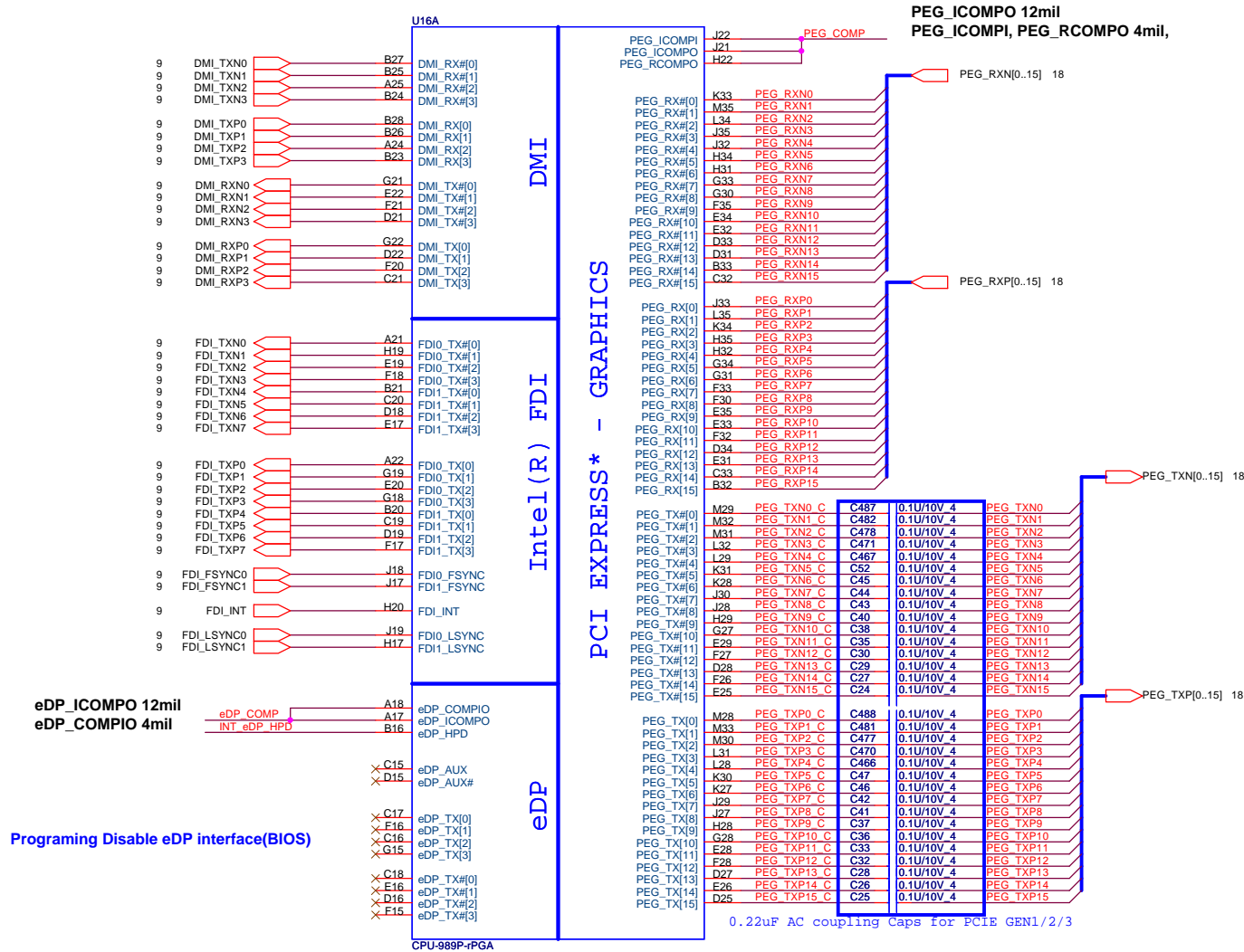
V02A/R01A DIS BLOCK DIAGRAM



power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation

+1.05V_PCH

R21 24.9/F 4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils

+1.05V_PCH

R47 24.9/F 4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

eDP Hot-plug (Disable)

+1.05V_PCH

R20 *10K_4_NC

INT_eDP_HPDI

CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

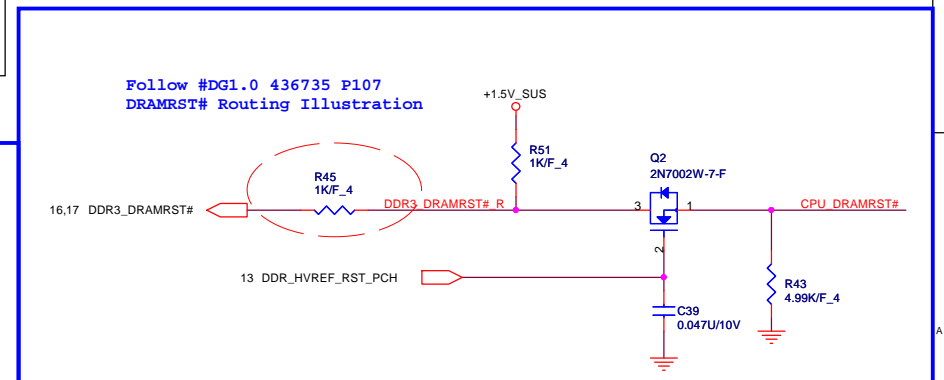
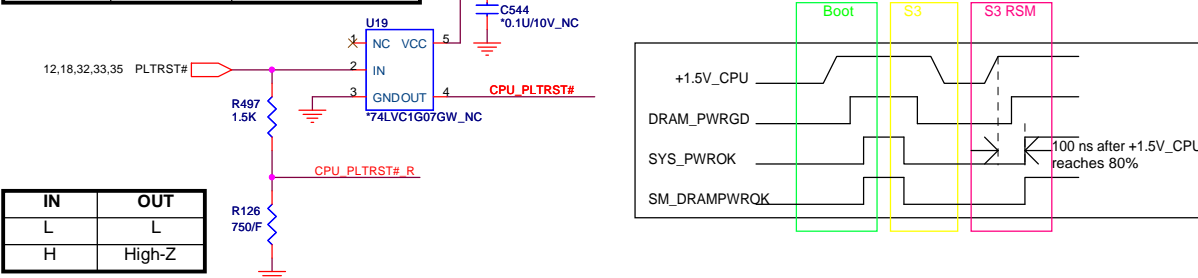
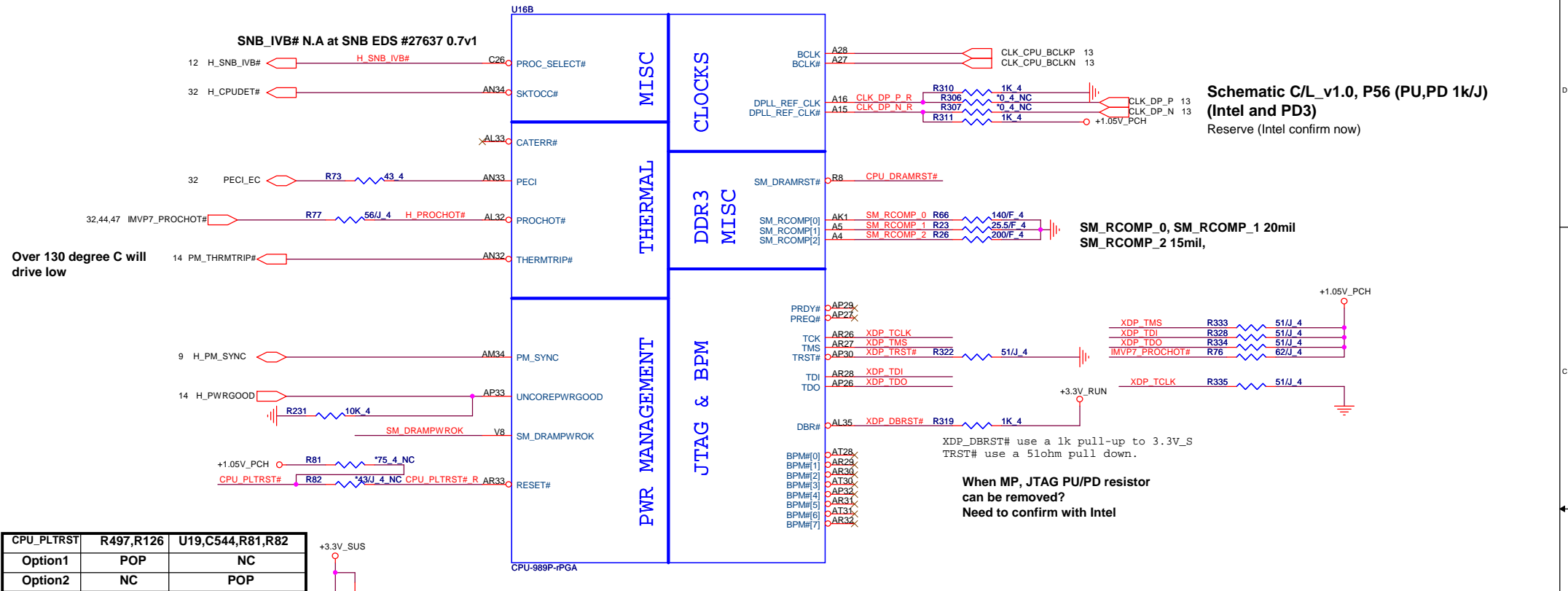


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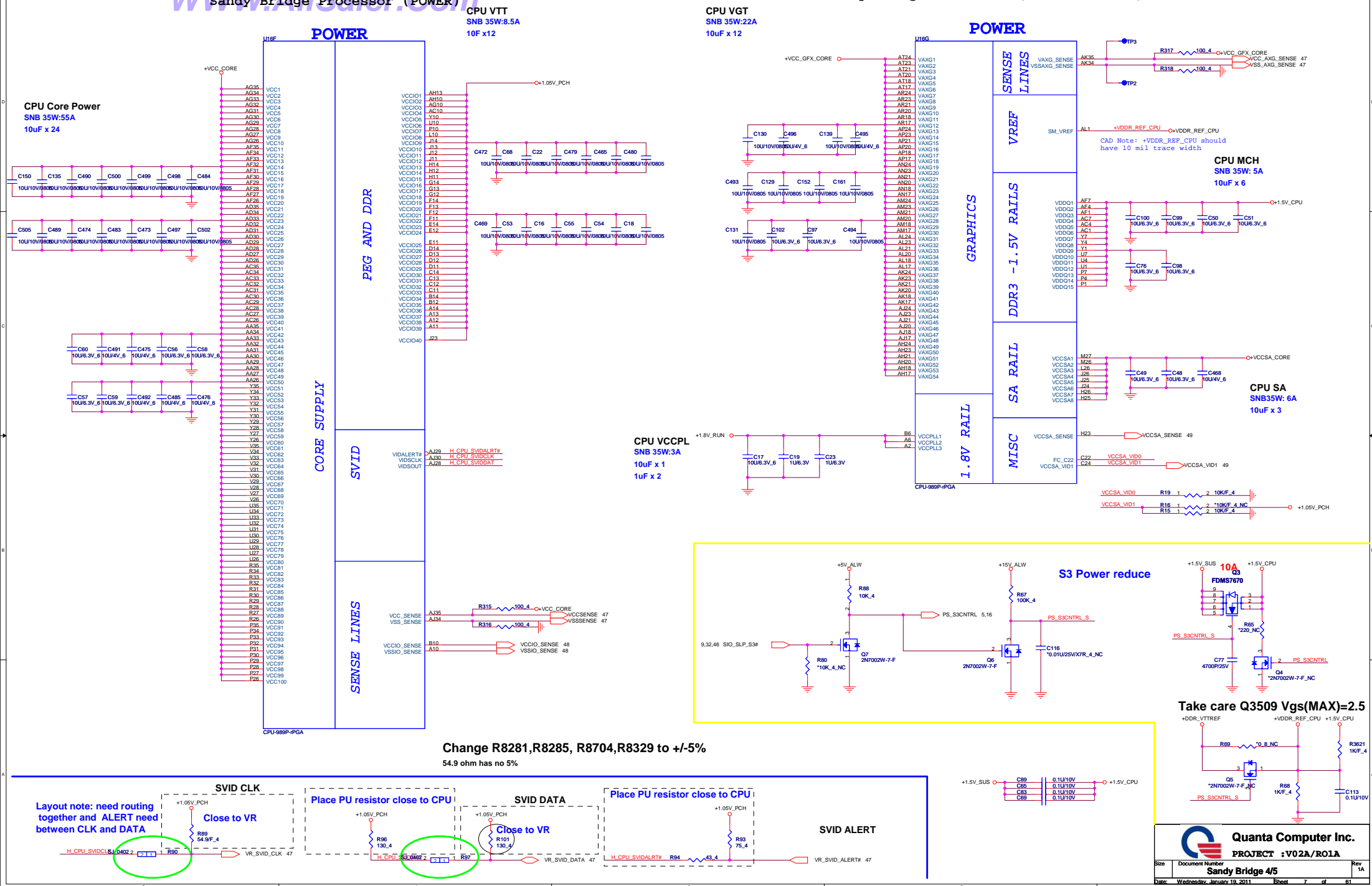
PROJECT : V02A/RO1A

Size	Document Number	Rev
	Sandy Bridge 1/5	1A
Date:	Wednesday, January 19, 2011	Sheet 4 of 61

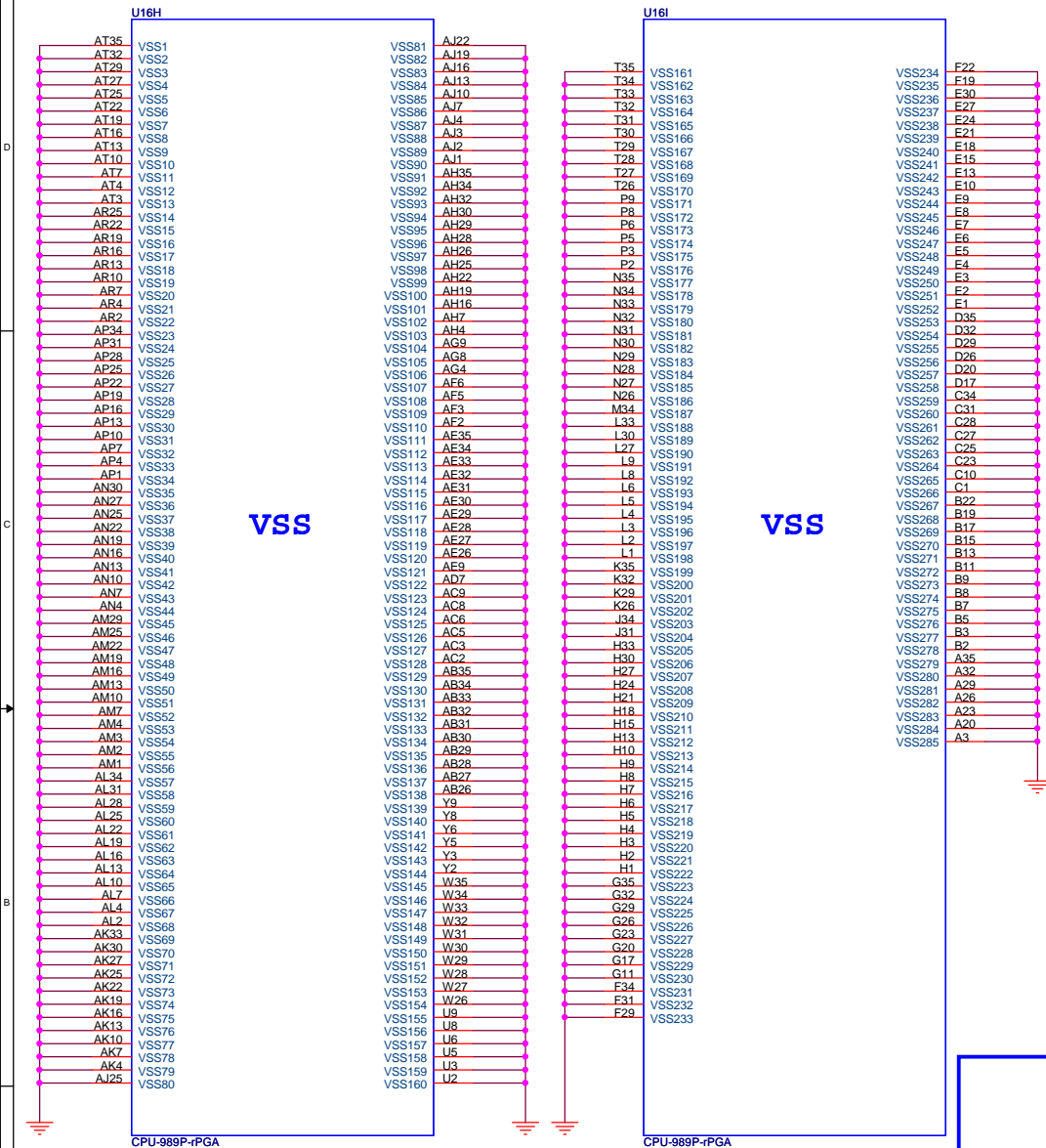
Sandy Bridge Processor (CLK,MISC,JTAG)



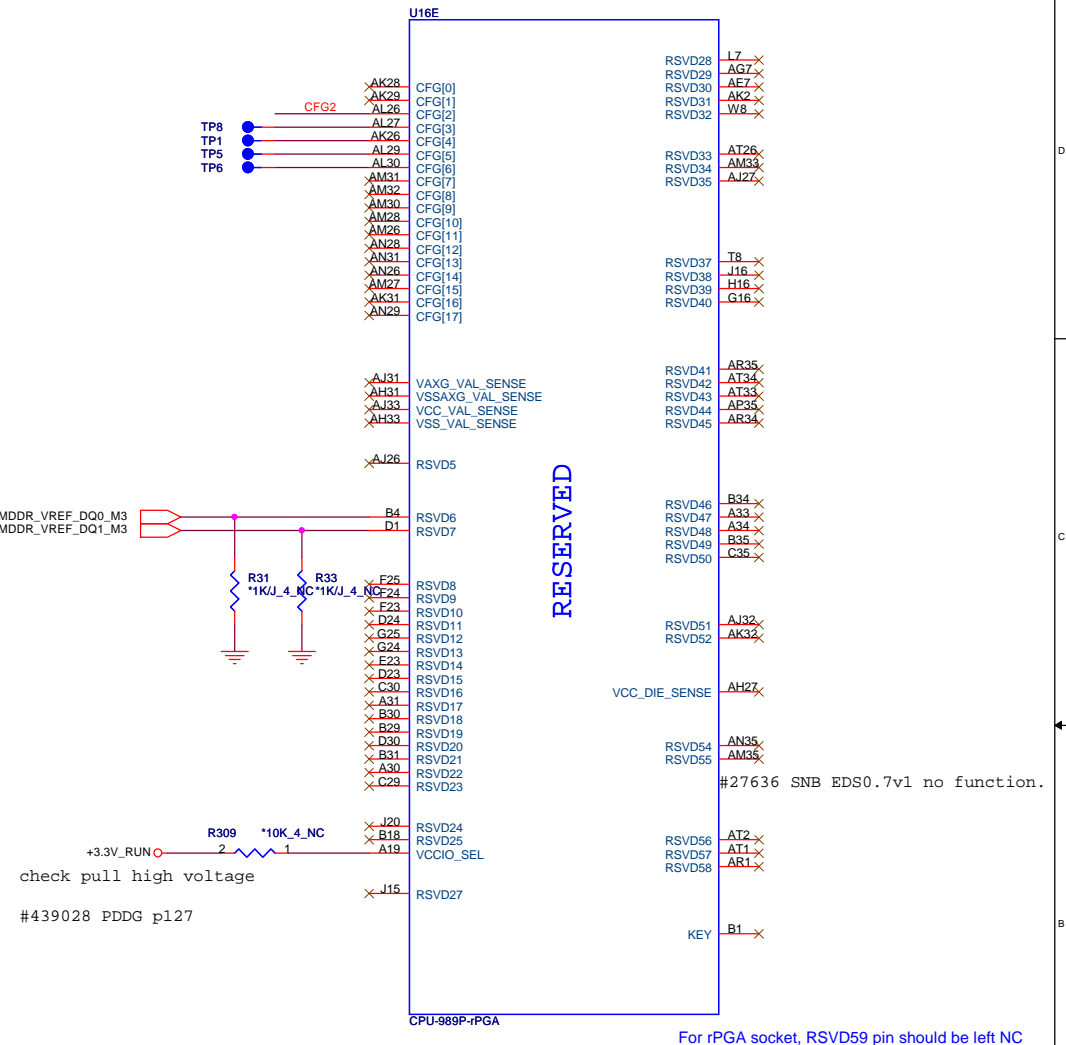




Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



For rPGA socket, RSVD59 pin should be left NC

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

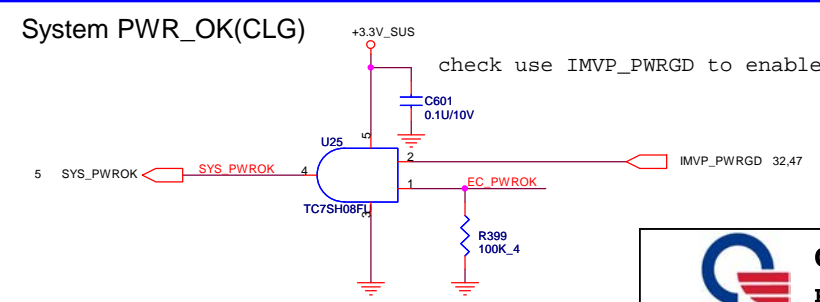
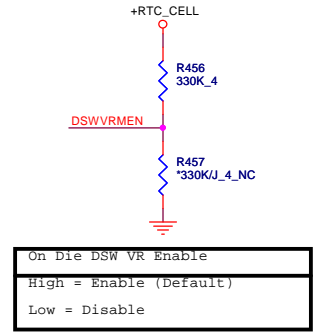
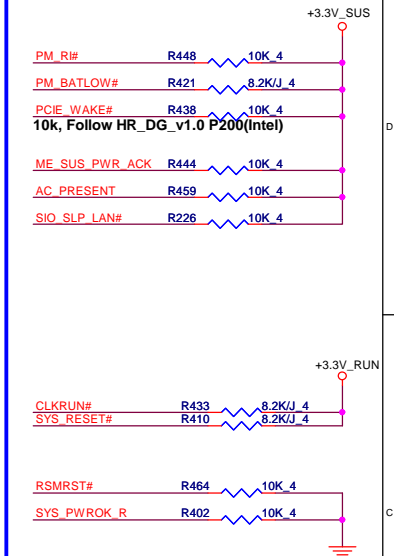
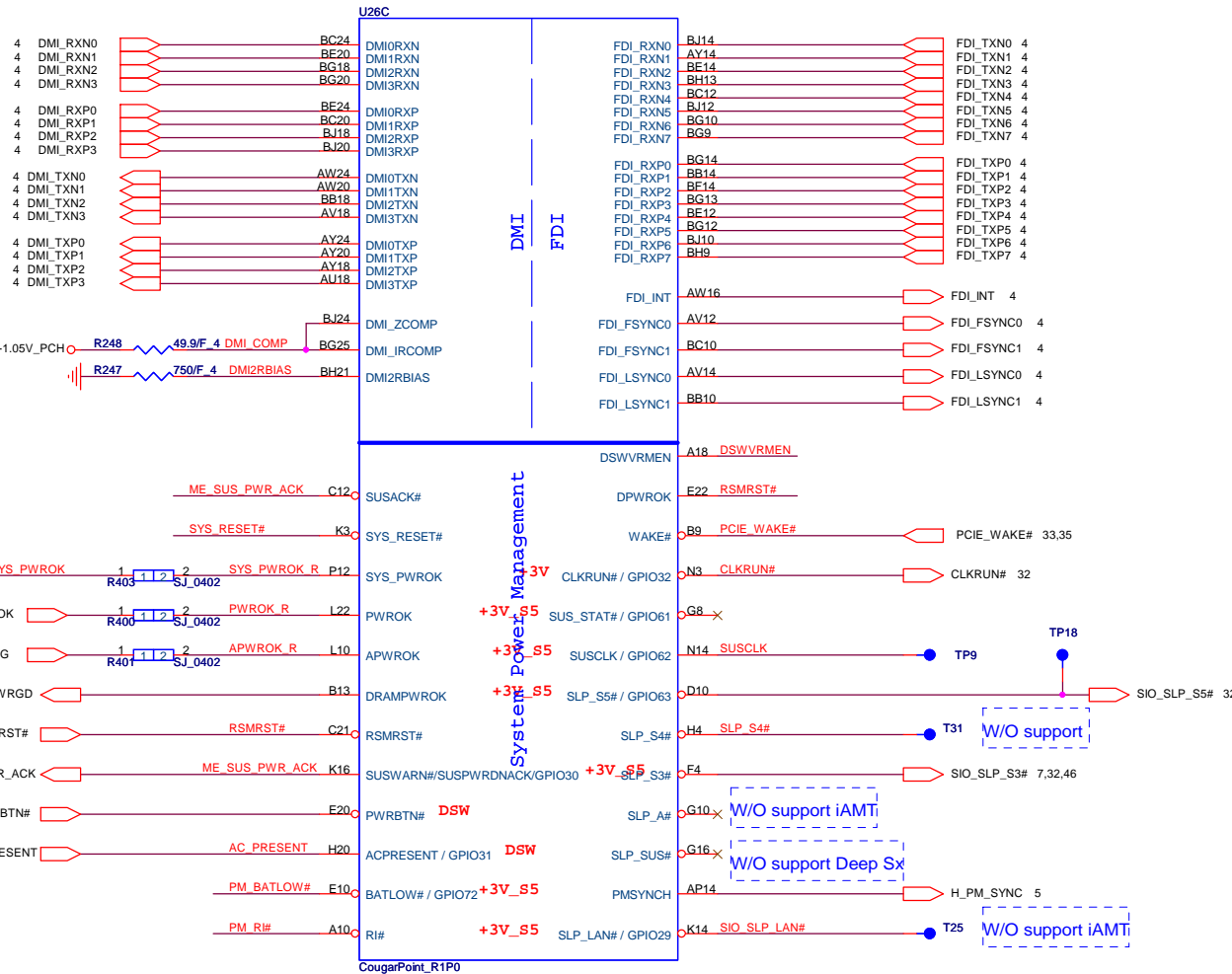


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PROJECT : V02A/R01A

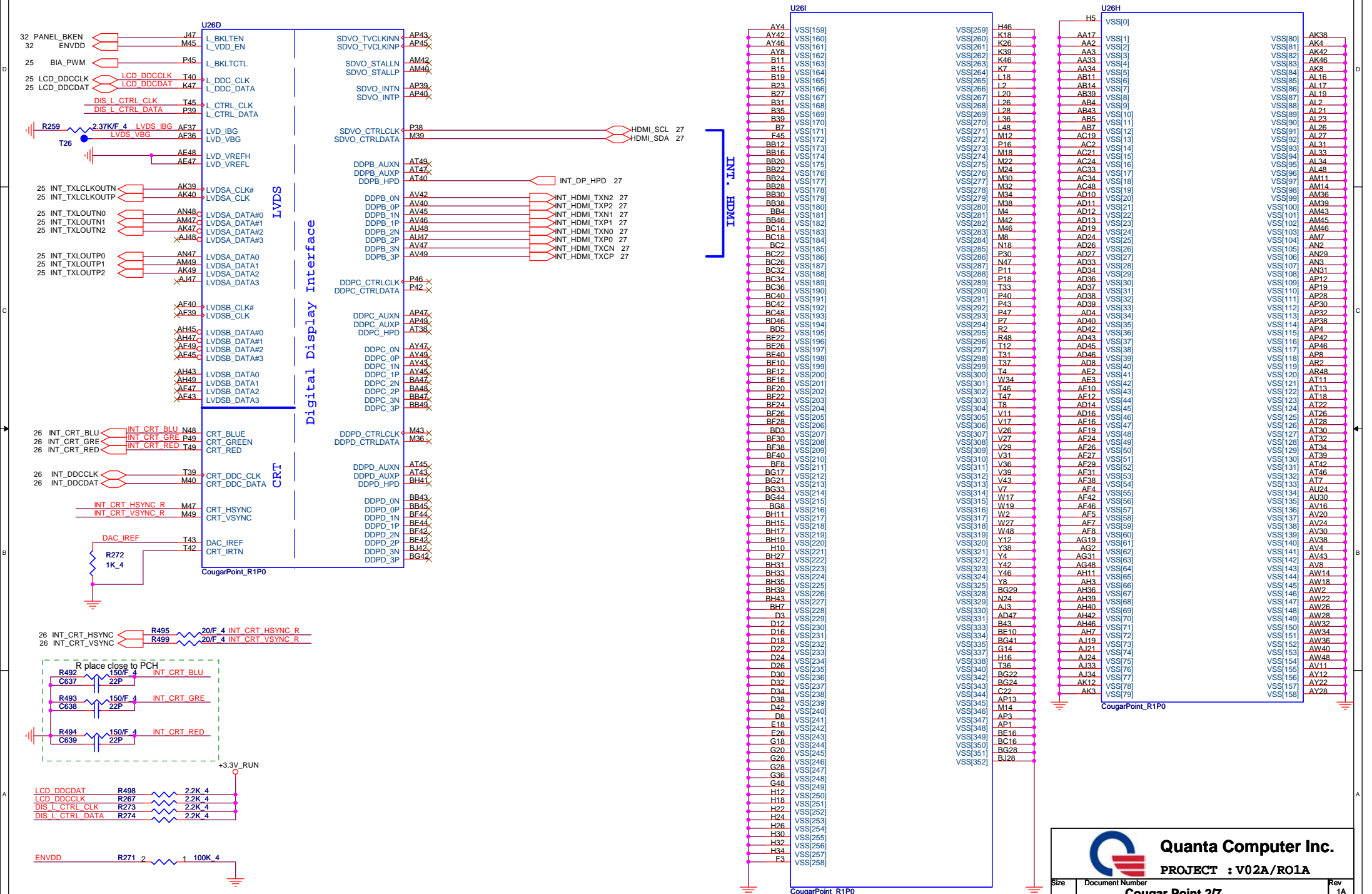
Sandy Bridge 5/5

Size	Document Number	Rev
	Sandy Bridge 5/5	1A
Date:	Wednesday, January 19, 2011	Sheet 8 of 61

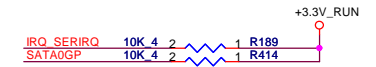
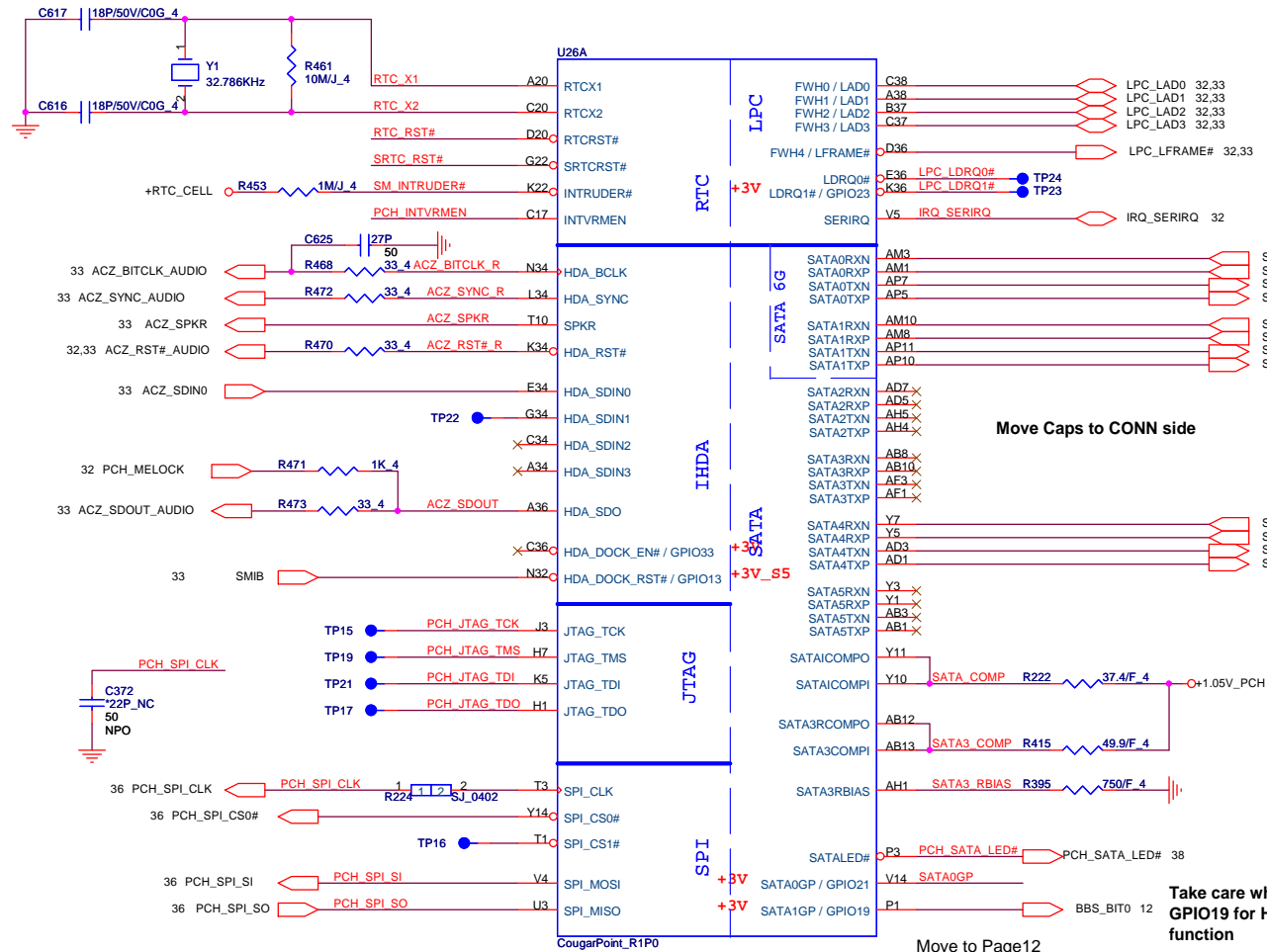


Cougar Point (LVDS,DDI)

Cougar Point (GND)

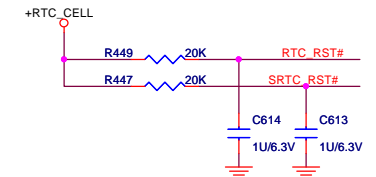
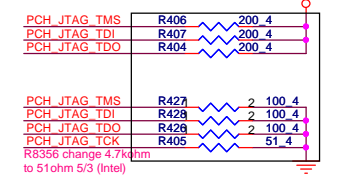


Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



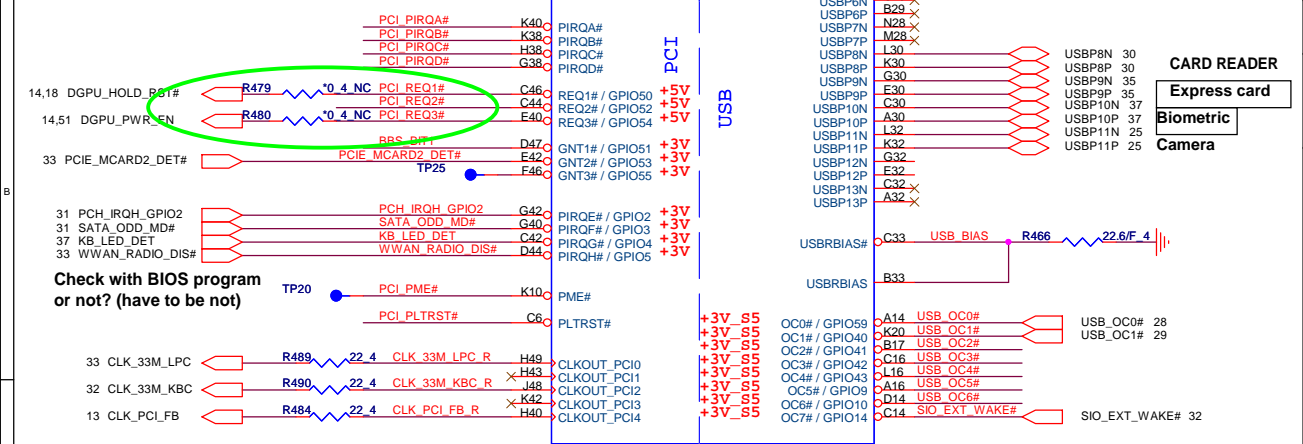
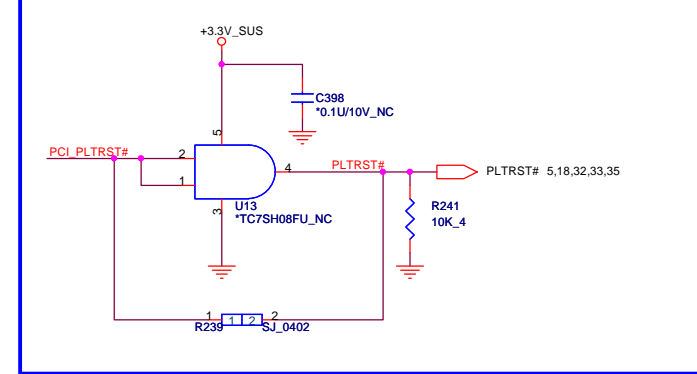
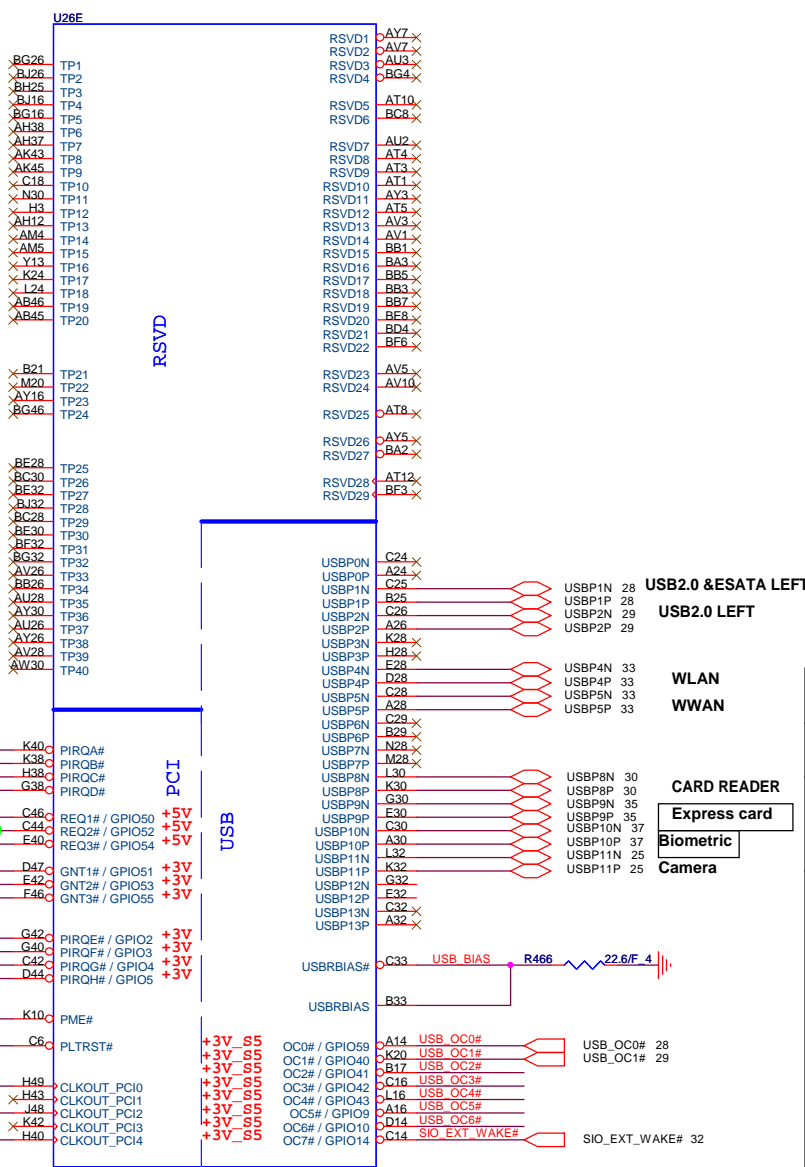
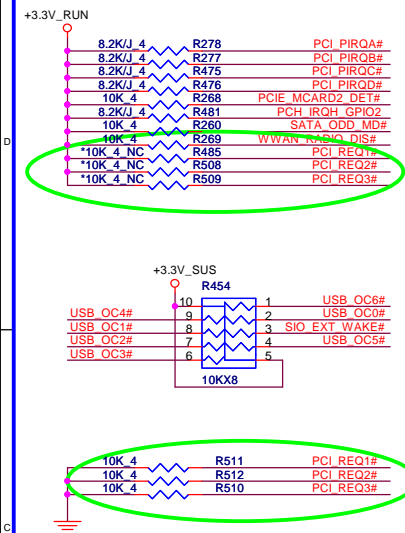
PCH Strap Table

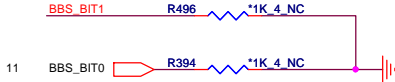
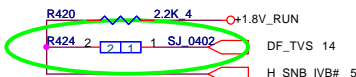
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS \rightarrow R413 \rightarrow *1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS \rightarrow R474 \rightarrow *1K 4 NC ACZ_SDO
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL \rightarrow R455 \rightarrow 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS \rightarrow R469 \rightarrow 1K 4 ACZ_SYNC_R

PCI/USBOC# Pull-up(CLG)

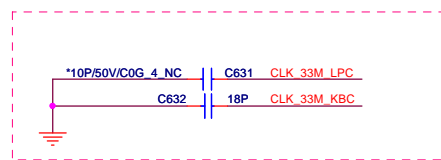
Cougar Point-M (PCI,USB,NVRAM)

PLTRST#(CLG)



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
			Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]									
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
												
CheckList_1.0 p58; HR_v1.0 p450												

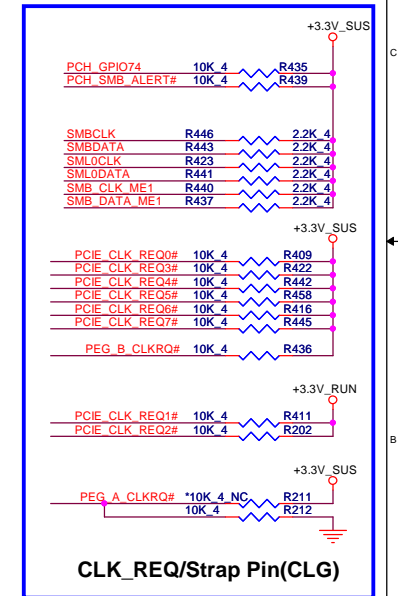
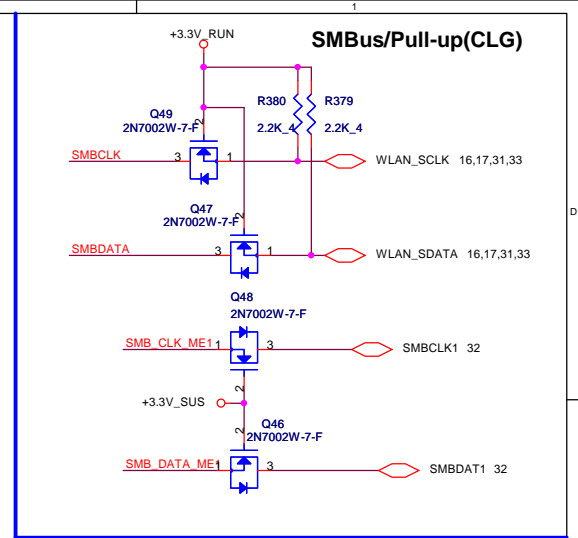
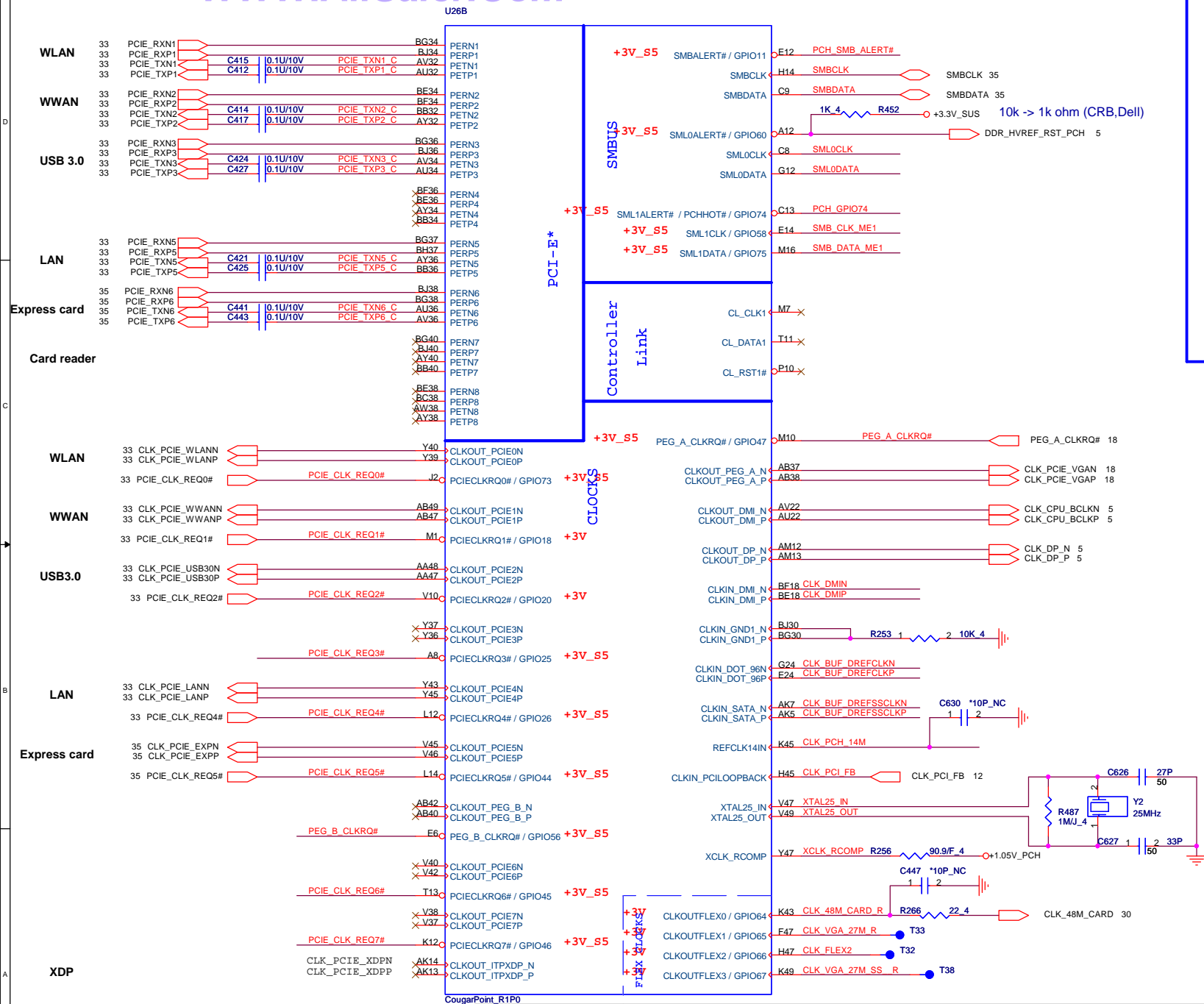
Check CLKOUT if Skew requirement?



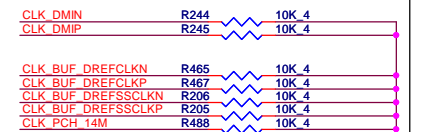
Quanta Computer Inc.

PROJECT : V02A/RO1A

Cougar Point 4/7



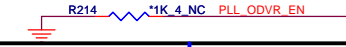
Stuff for Integrated CLK Gen Mode



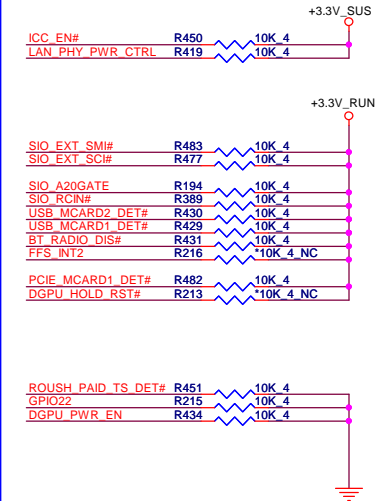
CougarPoint_R1P0	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 MHz output to SIO/EC / 24 MHz (Default)

Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



GPIO Pull-up/Pull-down(CLG)



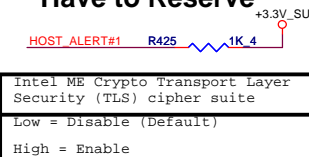
Add Description
in EC GPIO table
(keyboard
controller reset)

Check When Symbol Update (OK)

Can be del



Have to Reserve



MFG-TEST



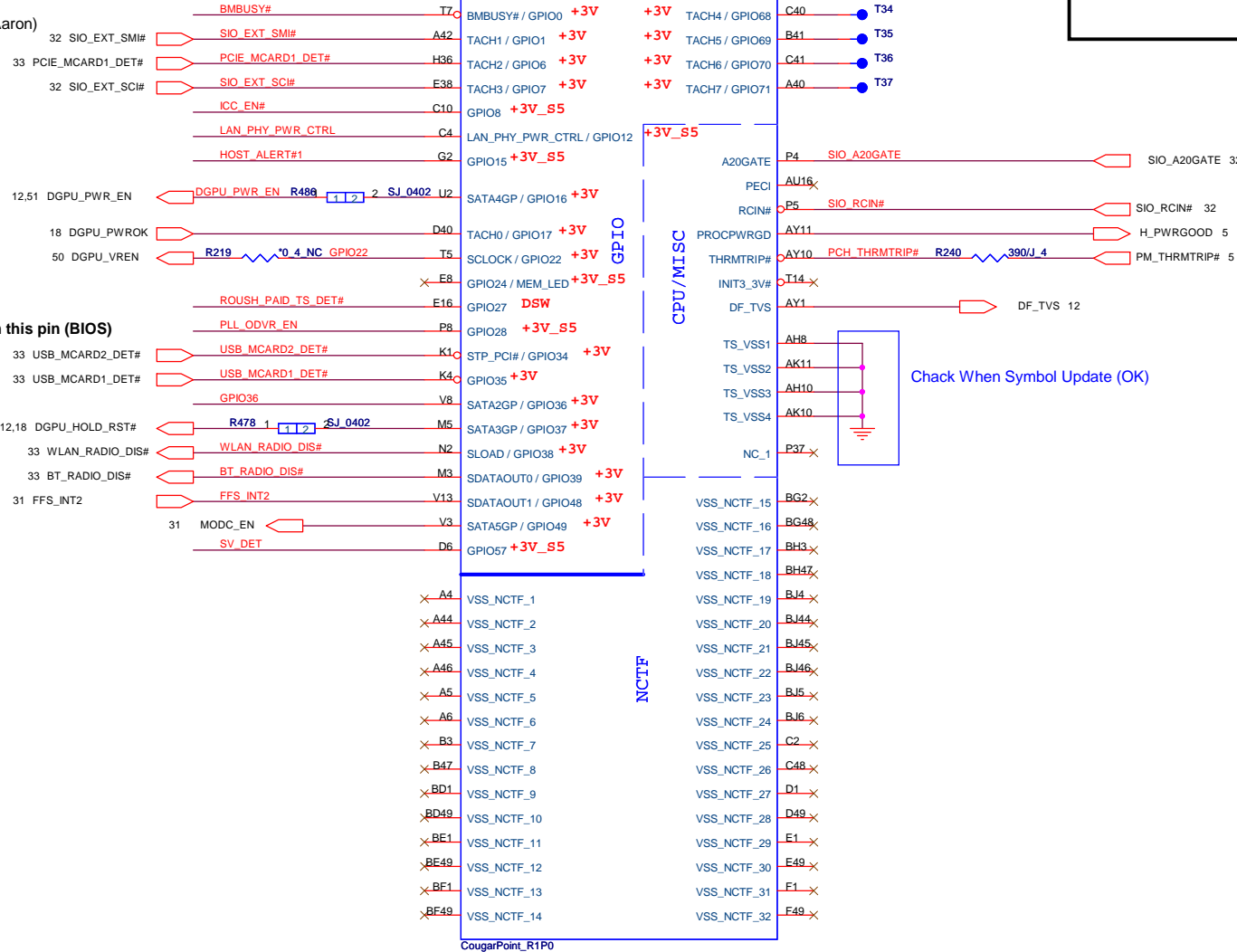
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PROJECT : V02A/RO1A

Cougar Point 6/7

Size	Document Number	Rev
		1A
Date:	Wednesday, January 19, 2011	Sheet 14 of 61

change to GPIO14 (Aaron)



SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

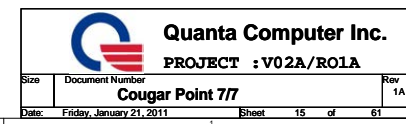


BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 KΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm pull-down for validation purpose

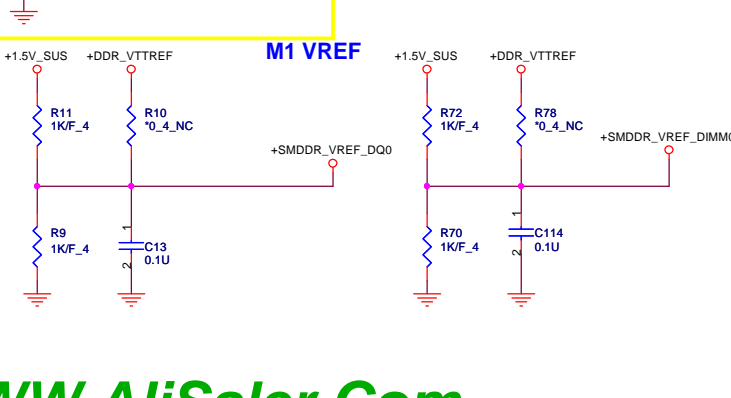
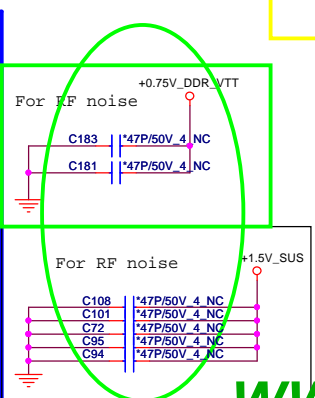
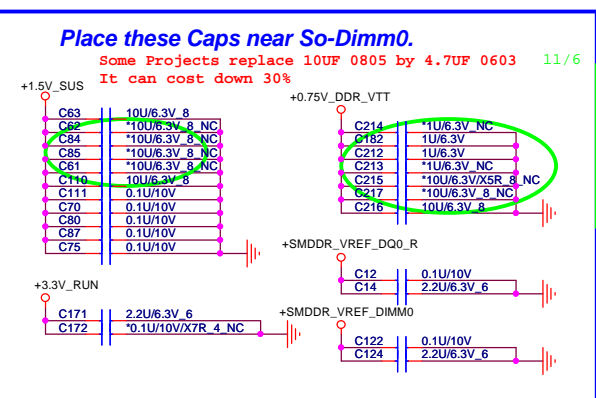
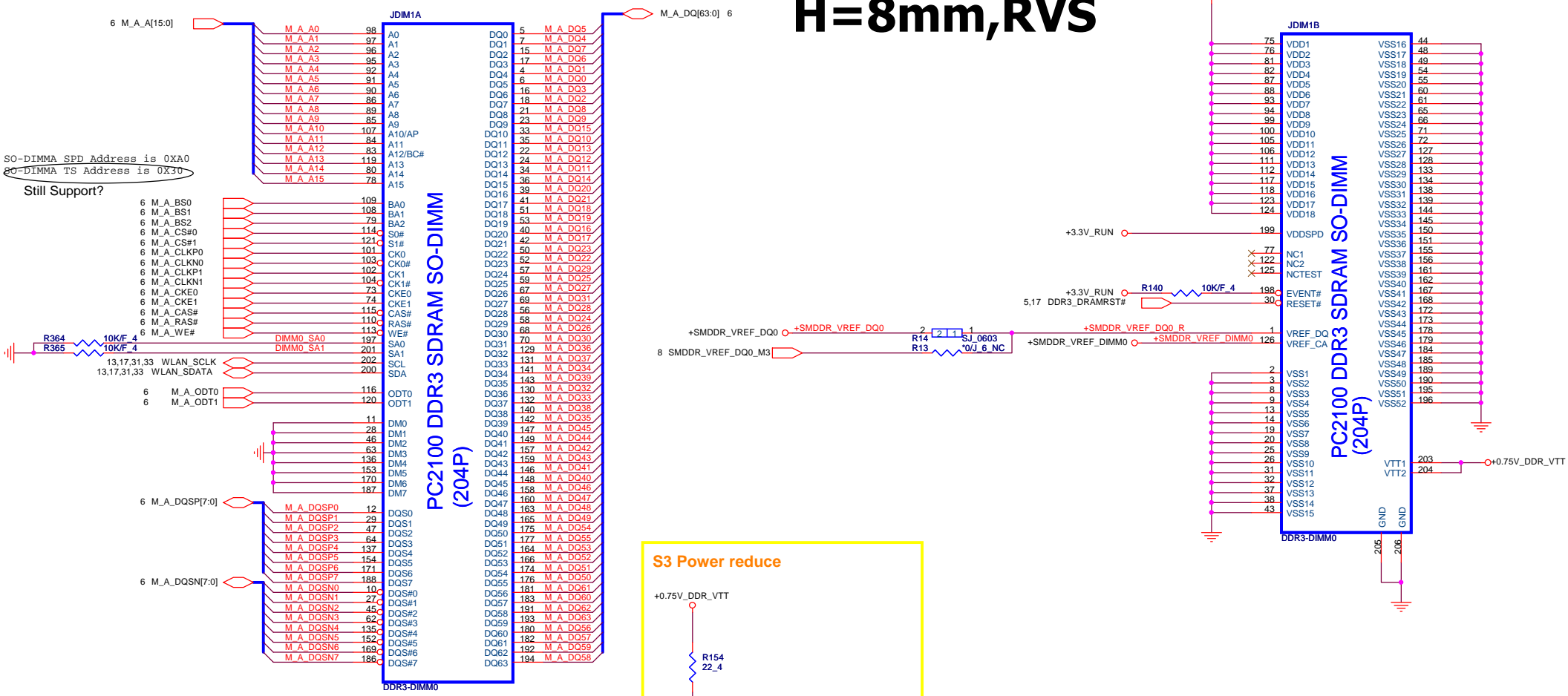
DMI TERMINATION
VOLTAGE OVERRIDE

Low = Tx, Rx terminated to
same voltage (DC Coupling Mode)
(DEFAULT)

Cougar Point (POWER)




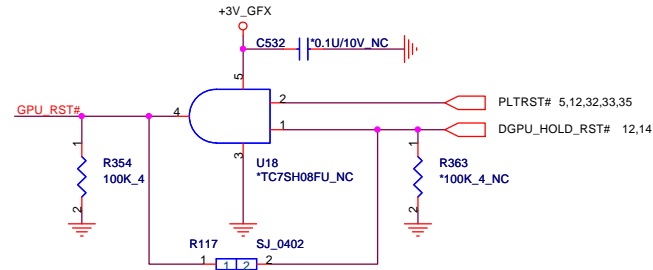
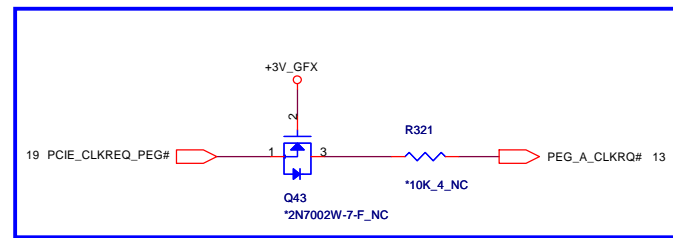
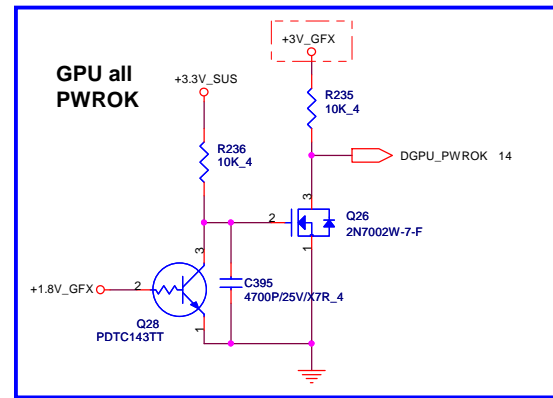
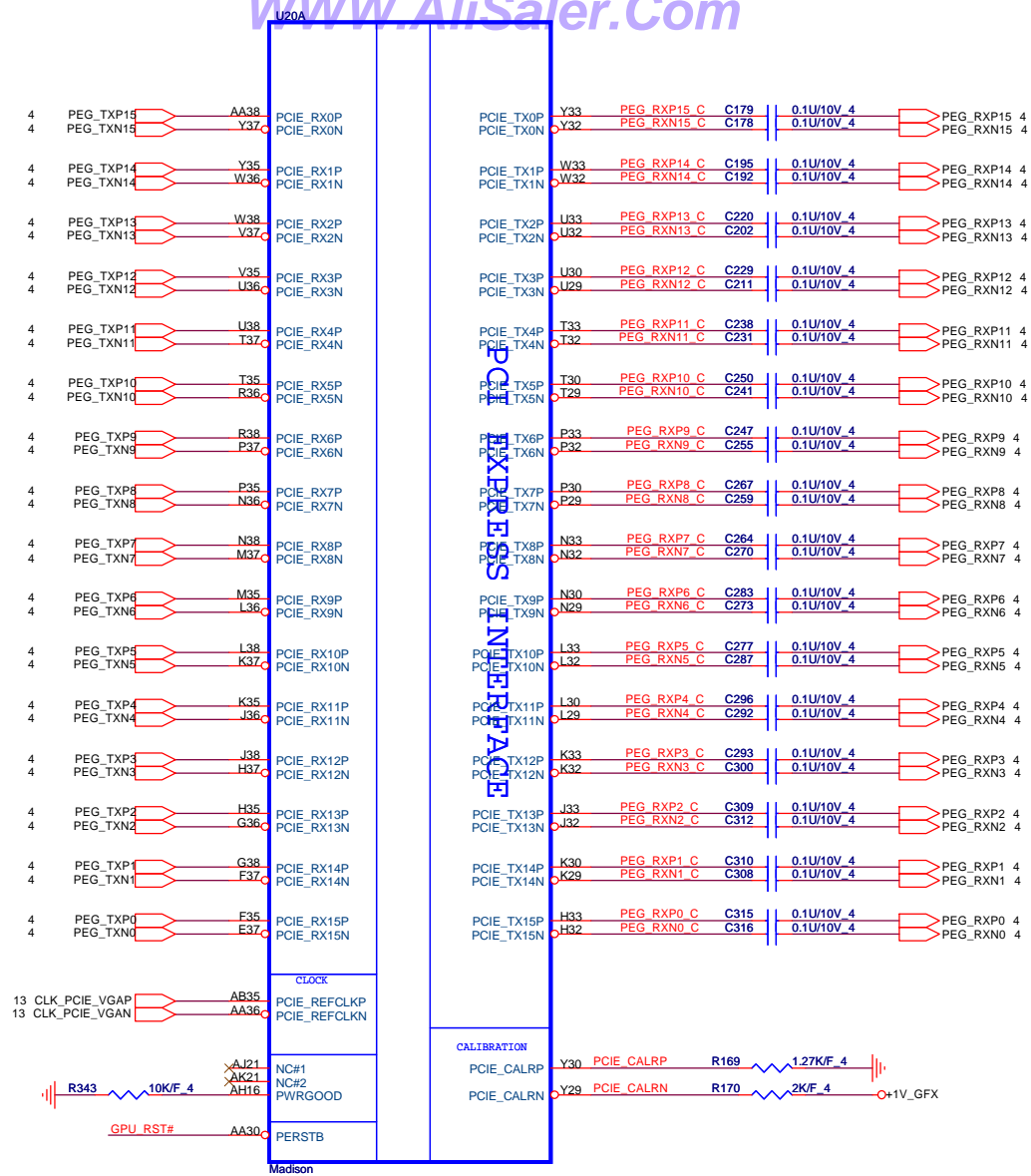
H=8mm,RVS



WWW.AliSaler.Com



 Quanta Computer Inc. PROJECT : V02A/RO1A		
Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date:	Wednesday, January 19, 2011	Sheet 17 of 61



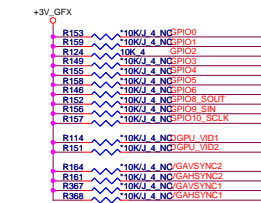
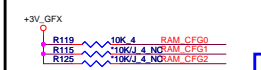
Quanta Computer Inc.
PROJECT : V02A/RO1A

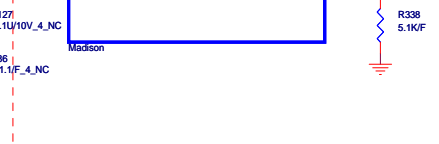
Size	Document Number	Rev
	N11M-GE2 (PCIE I/F) 1/5	1A
Date:	Wednesday, January 19, 2011	Sheet 18 of 61

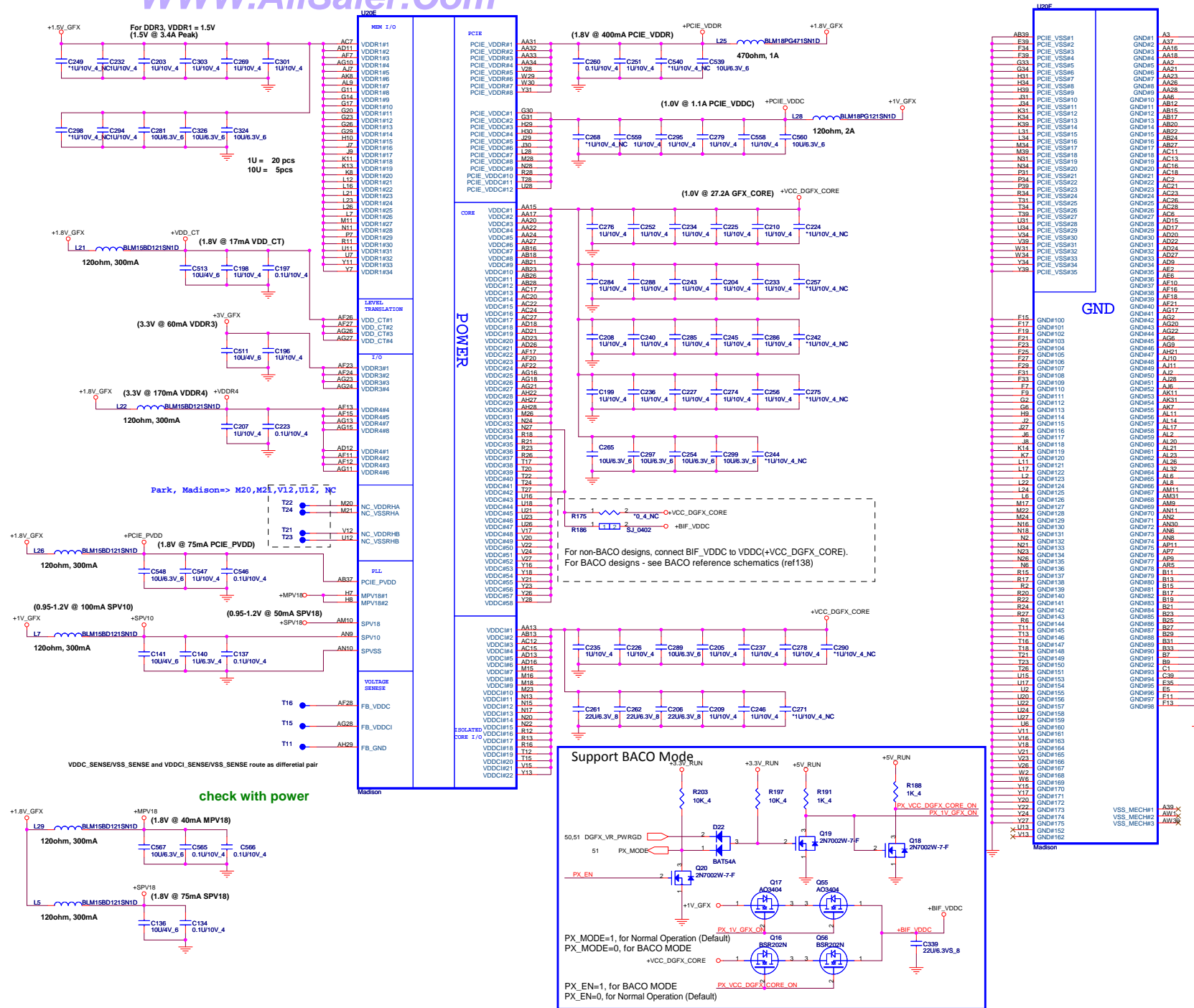
CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGA_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0







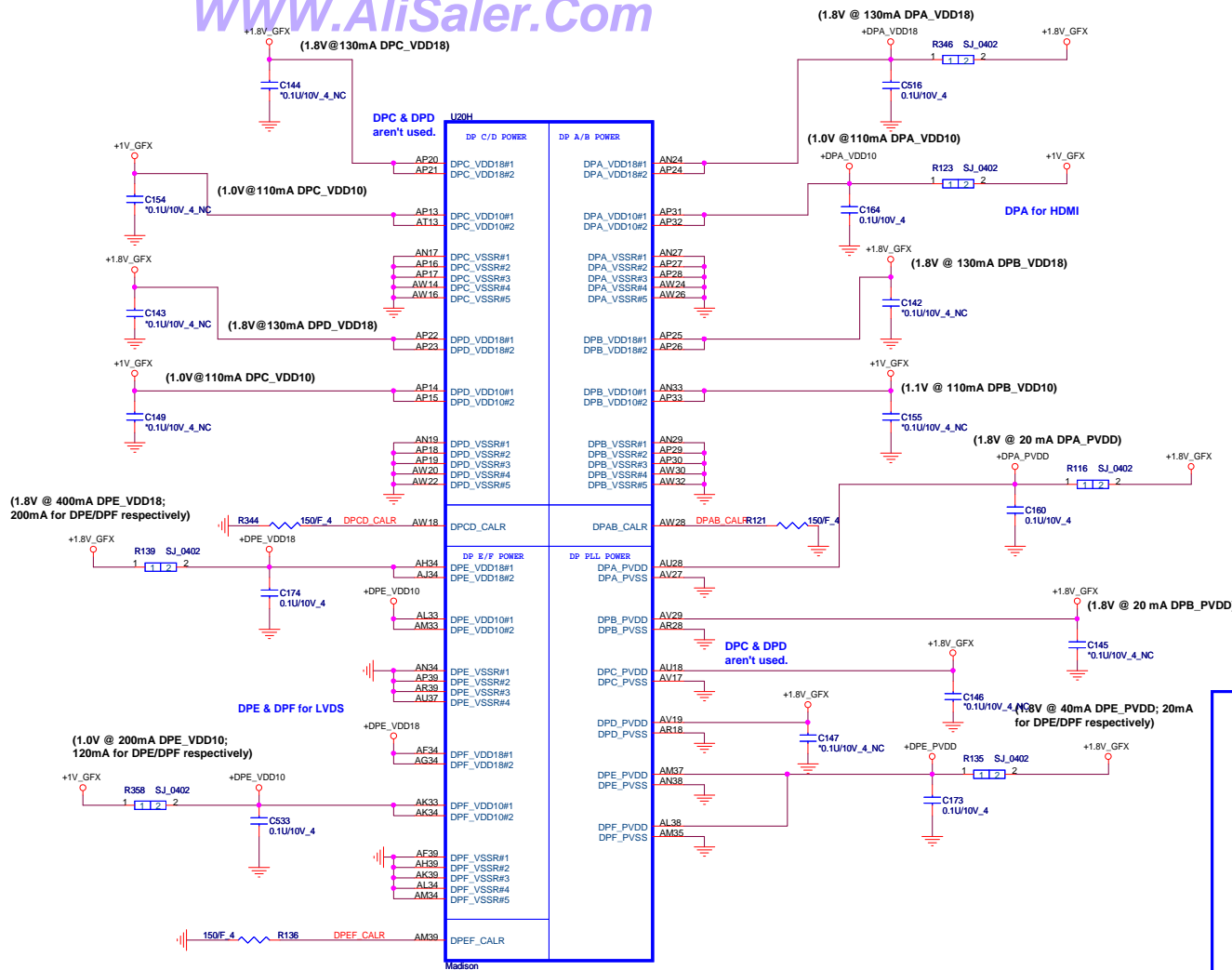
PowerXpress control signal for Madison and Park only
If not used, can be disconnected. (AL21 pin)

PX_EN = LOW, turn on
PX_EN = HIGH, turn off

Reserve for support BACO mode

PX_EN R113 10K_4

AL21 For PX_EN, refer to the BACO reference schematics for detail



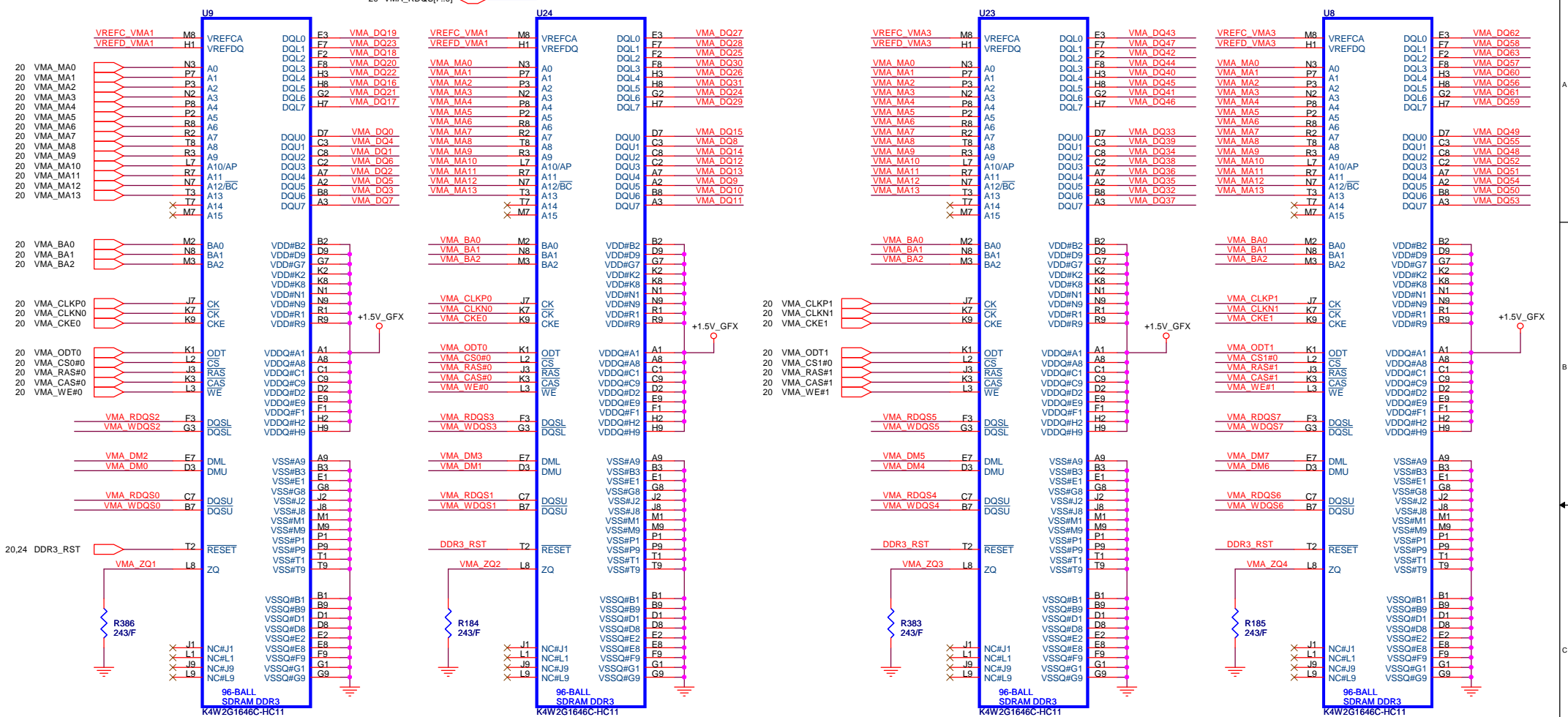
GPU Power Rail List

+1V_GFX=>	+1.8V_GPU=>
+DPA_VDD10	+A2VDDQ
+SPV10	+AVDD
+DPE_VDD10	+DPA_PVDD
+DPLL_VDDC	+DPA_VDD18
+PCIE_VDDC	+DPE_PVDD
	+DPE_VDD18
	+DPLL_PVDD
	+MPV18
	+PCIE_PVDD
	+PCIE_VDDR
	+SPV18
	+TSVDD
	+VDD1DI
	+VDD2DI
	+VDD_CT
	+VDDR4

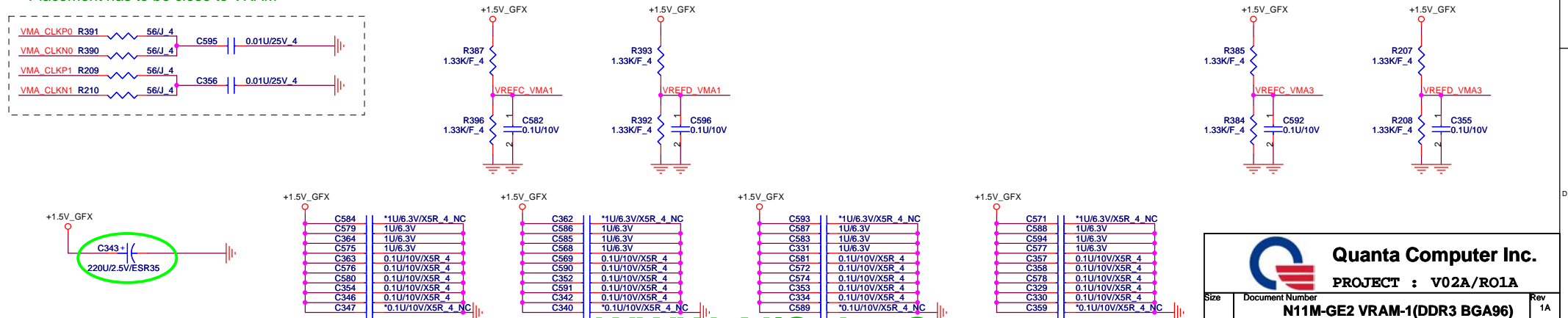
GPU Power-on sequence

- 1 => +3V_GFX
- 2 => +VCC_DGFX_CORE
- 3 => +1V_GFX
- 4 => +1.5V_GFX
- 5 => +1.8V_GFX
- 6 => dGPU_PWROK

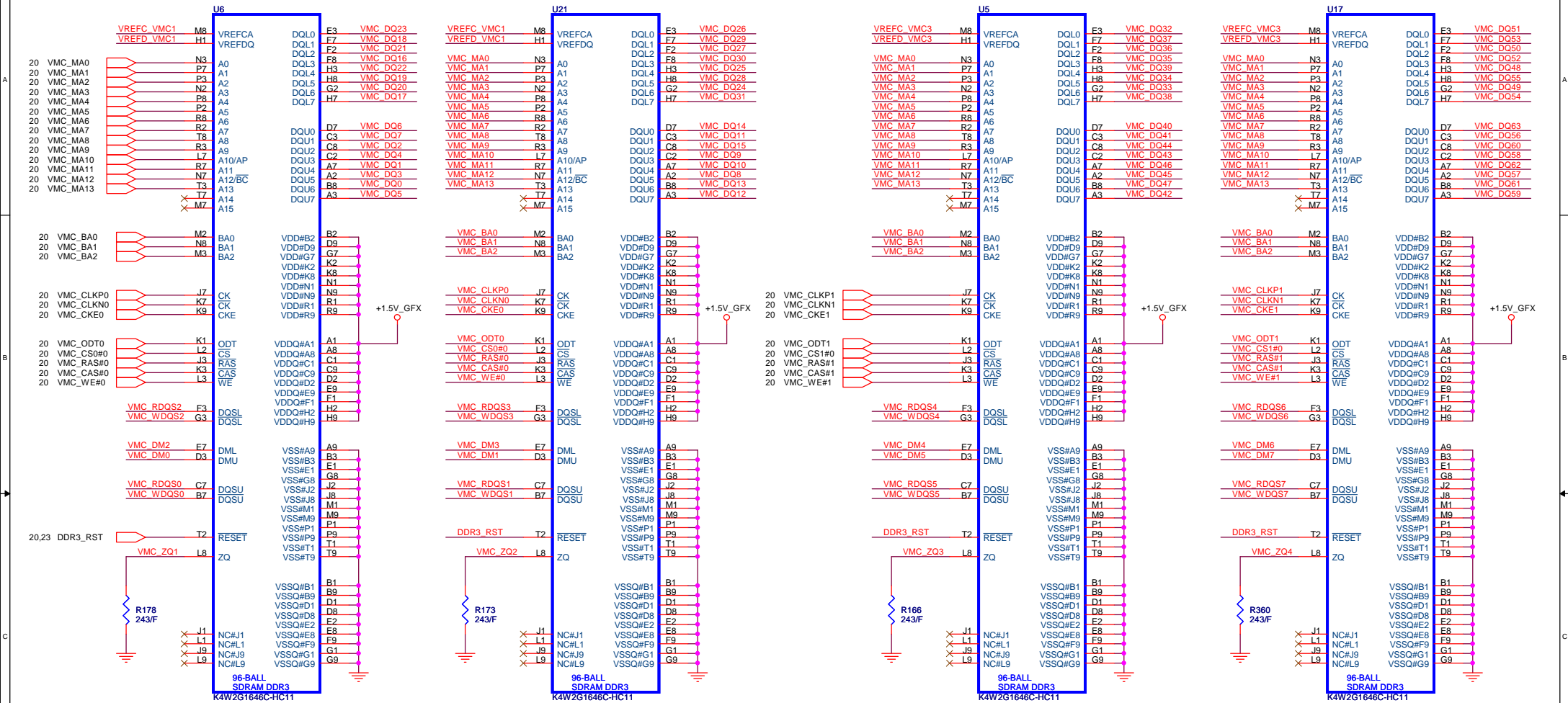
CHANNEL A: 1024MB DDR3



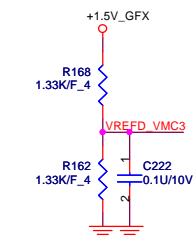
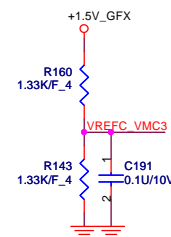
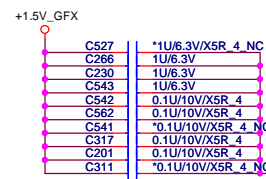
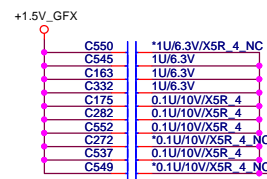
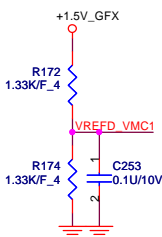
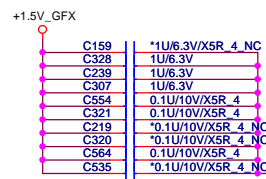
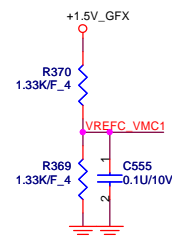
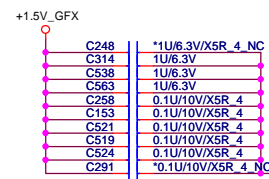
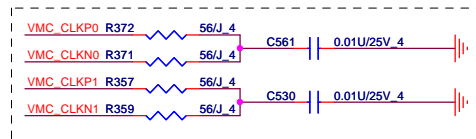
Placement has to be close to VRAM

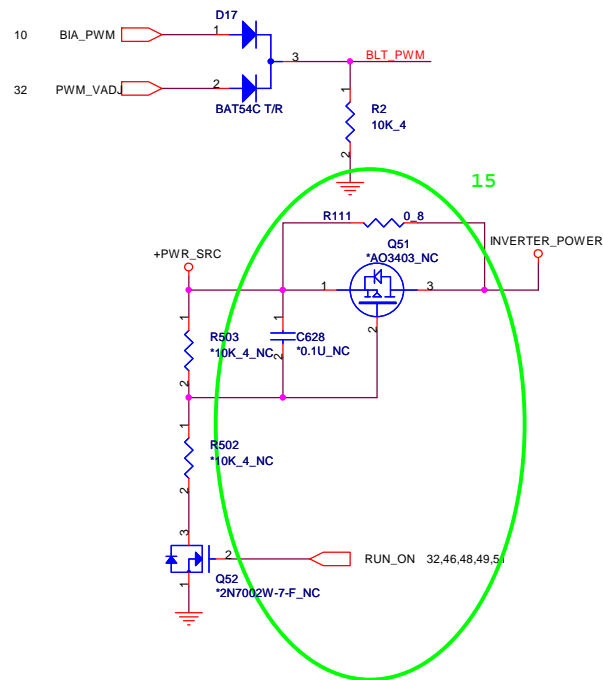
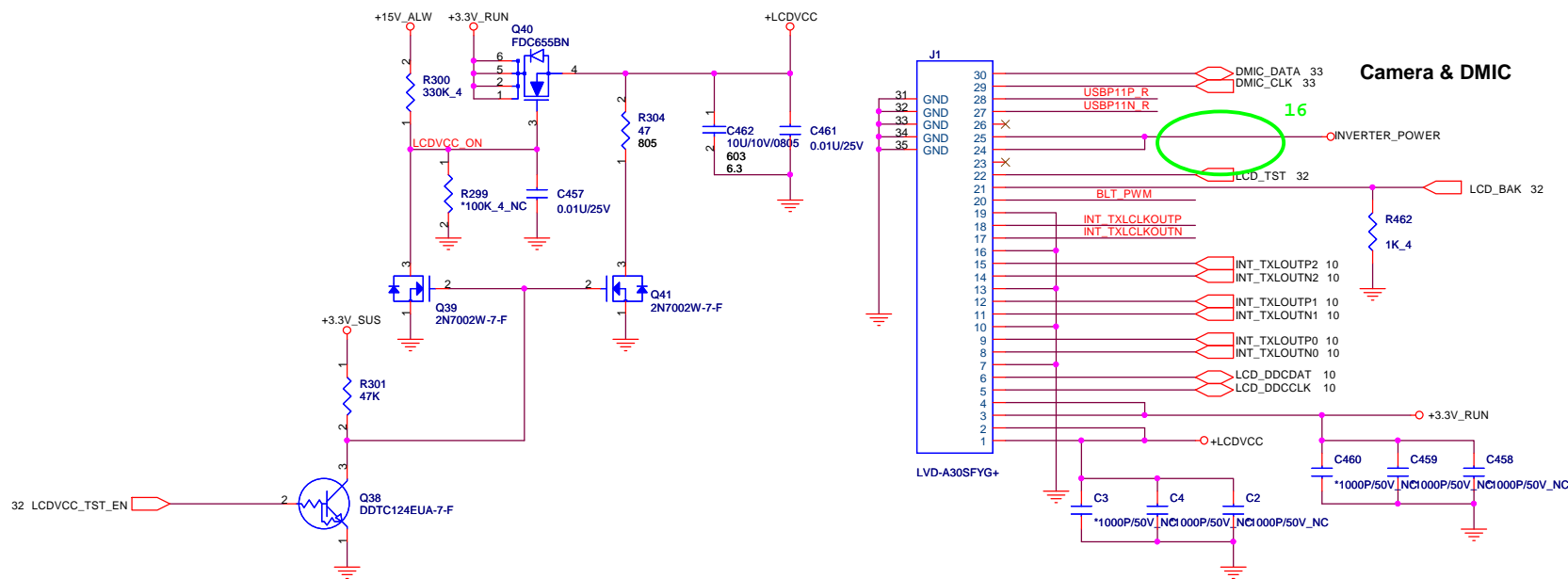


CHANNEL B: 1024MB DDR3

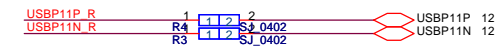
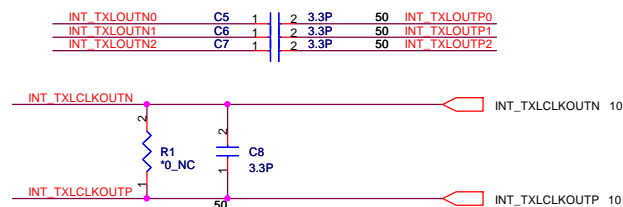


Placement has to be close to VRAM



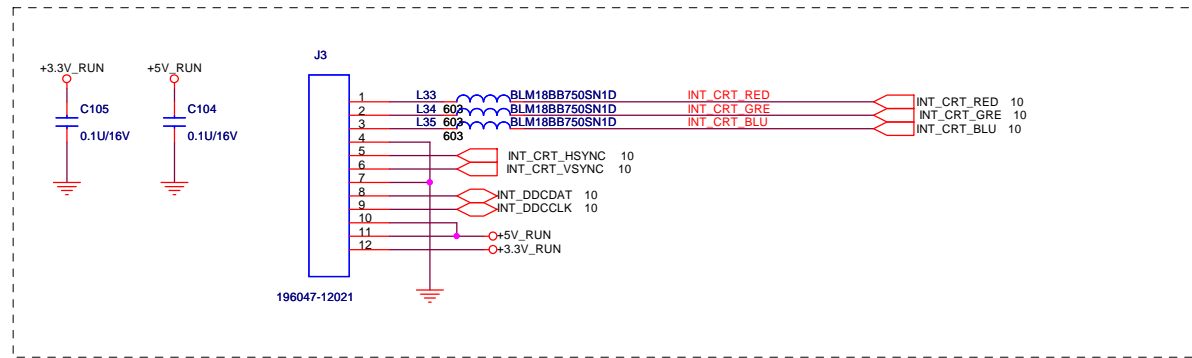


Shunt capacitors on LVDS for improving WWAN.

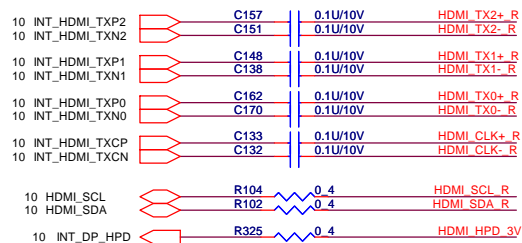


Quanta Computer Inc.
PROJECT : V02A/RO1A

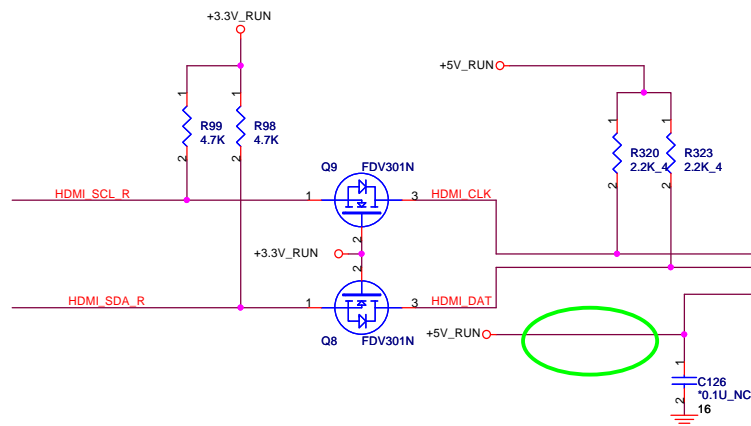
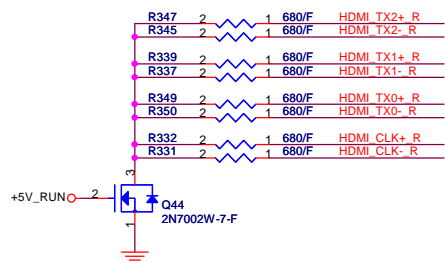
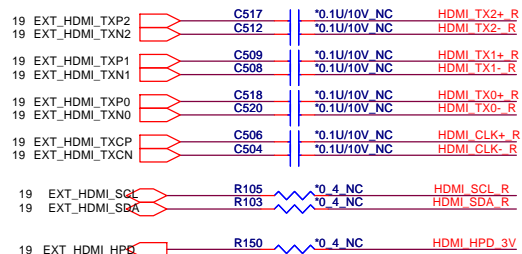
Size	Document Number	Rev
	LVDS CONN	1A
Date:	Wednesday, January 19, 2011	Sheet 25 of 61



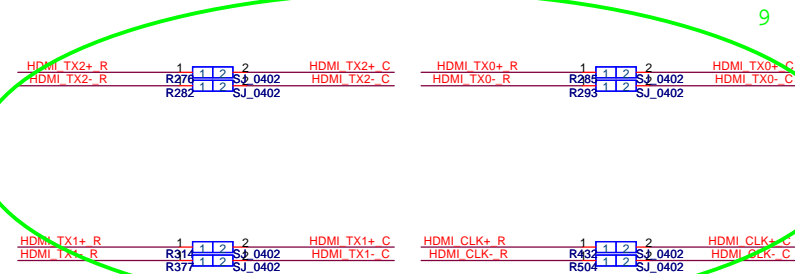
UMA HDMI



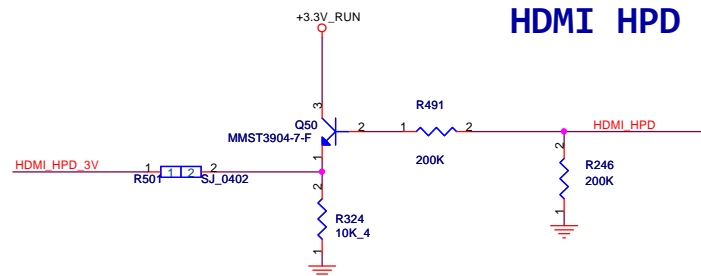
DIS HDMI



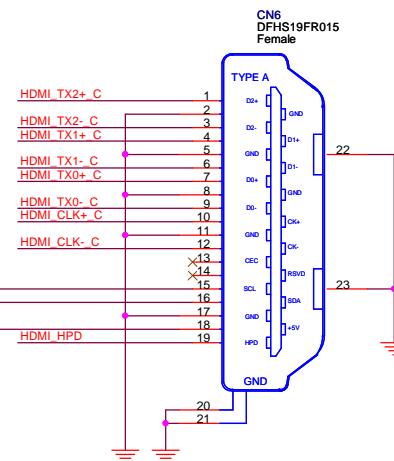
Reserve for EMI and close to HDMI CONN



HDMI HPD



HDMI Conn.



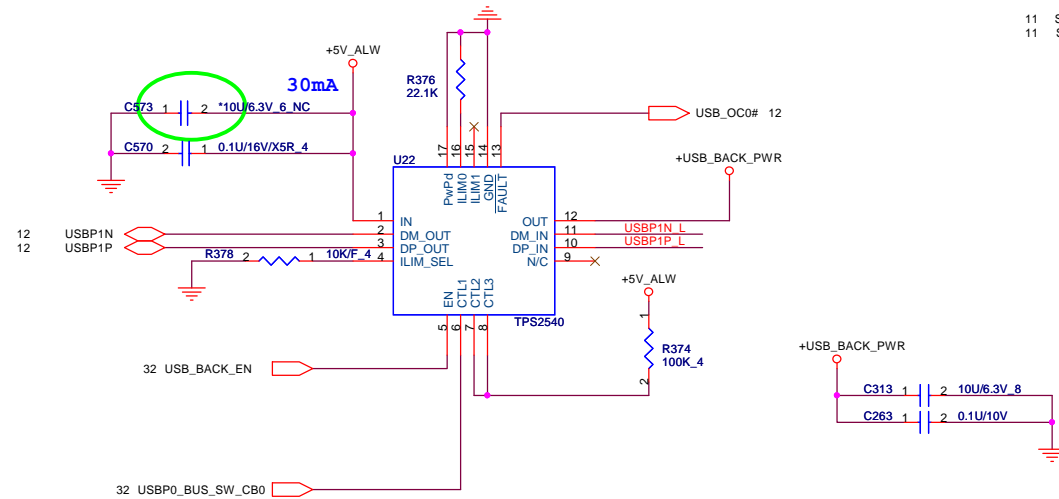
Quanta Computer Inc.

PROJECT : V02A/RO1A

HDMI CONN

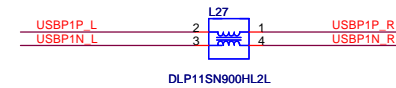
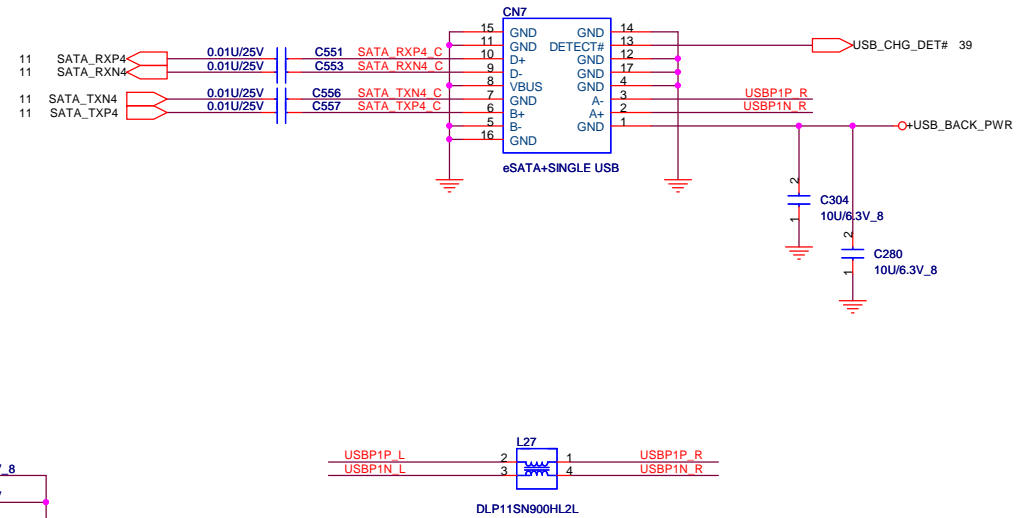
ESATA + USB Conn + Power share

S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R8224	mA	
OC	100k ohm	480	
limitation	22.1k ohm	2171	Applied Now



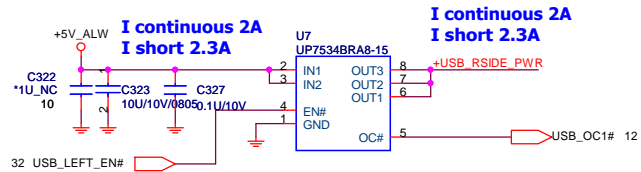
Quanta Computer Inc.

PROJECT : V02A/RO1A

PUSB / ESATA

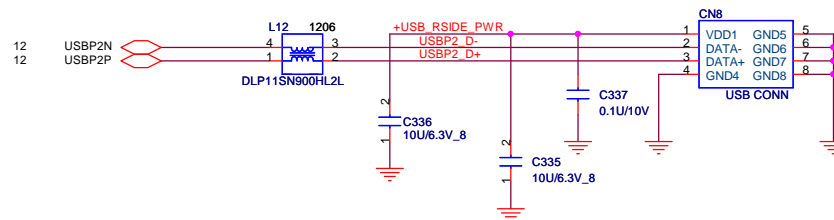
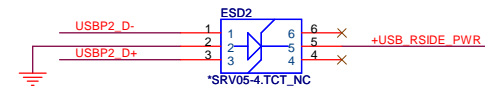
Size	Document Number	Rev
		1A
Date:	Wednesday, January 19, 2011	Sheet 28 of 61

UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

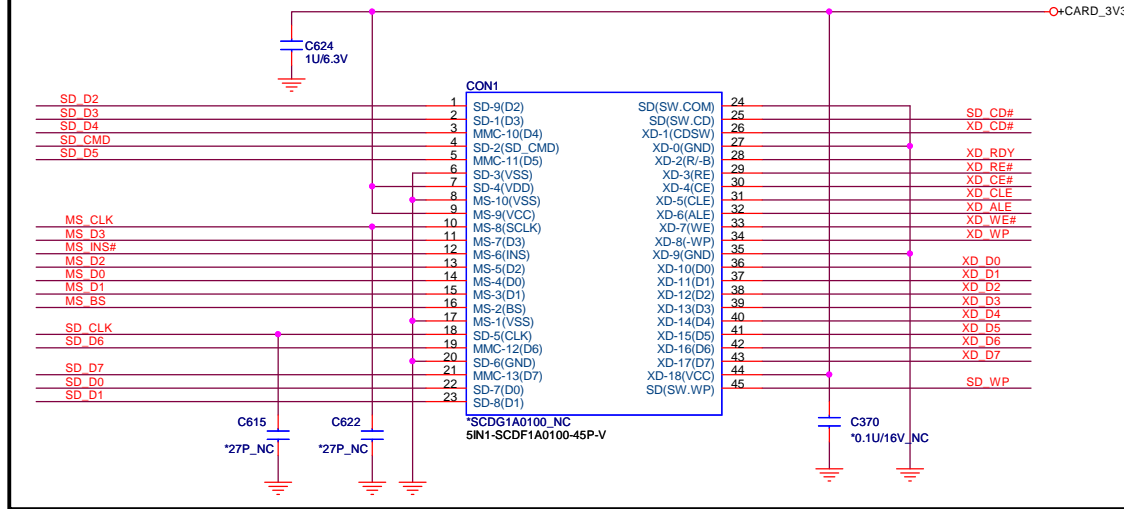


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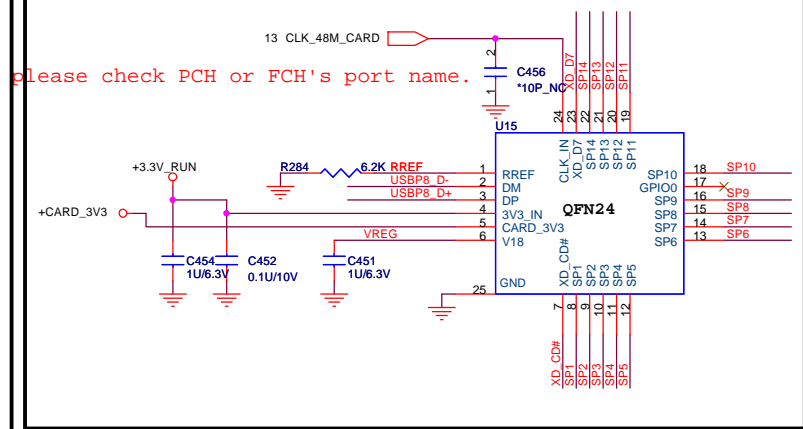
PROJECT : V02A/R01A

Size	Document Number	Rev
	USB 2.0	1A
Date:	Wednesday, January 19, 2011	Sheet 29 of 61

Inspiron

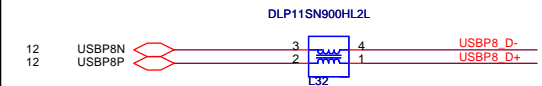


please check PCH or FCH's port name.

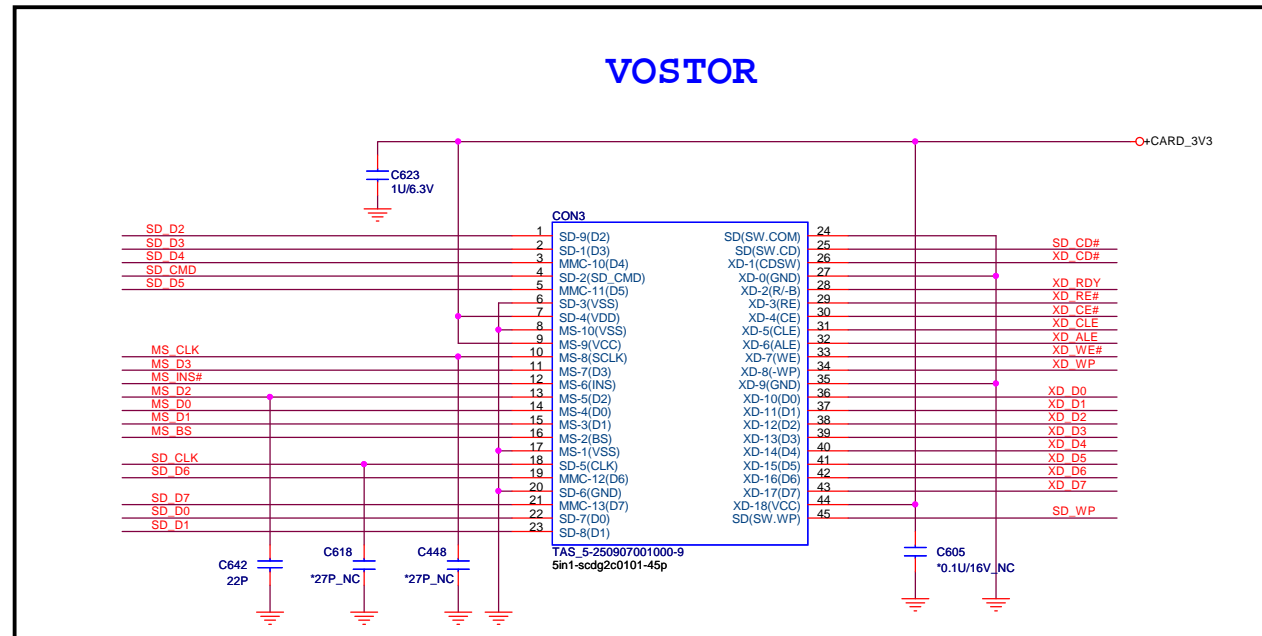


SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	MS D6
SP6	XD WE#	SD D6	MS D2
SP7	XD WP	SD CLK	MS D0
SP8	XD D0	SD D5	MS D0
SP9	XD D1	SD D4	MS D4
SP10	XD D2	SD D3	MS D1
SP11	XD D3	SD D2	MS D5
SP12	XD D4	SD D1	MS BS
SP13	XD D5	SD D0	
SP14	XD D6	SD D7	

Share Pin

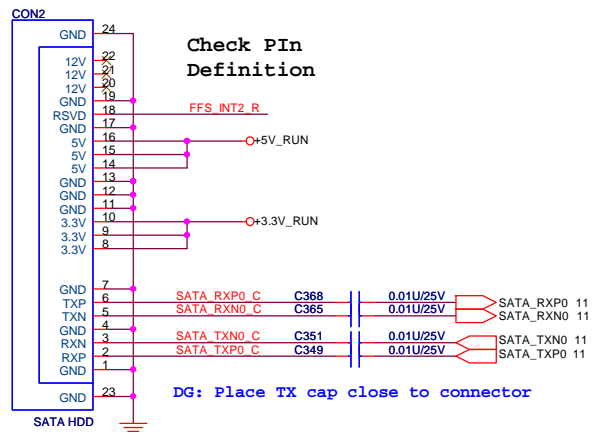


Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

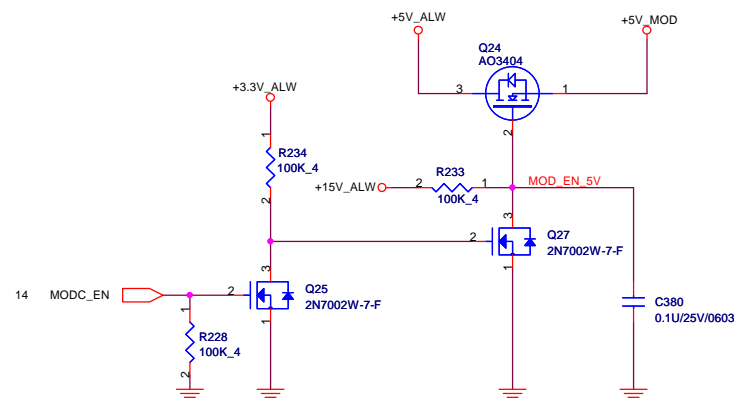
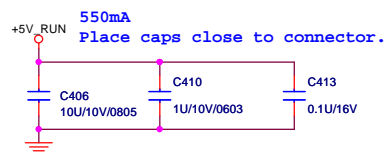
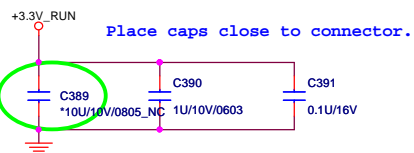
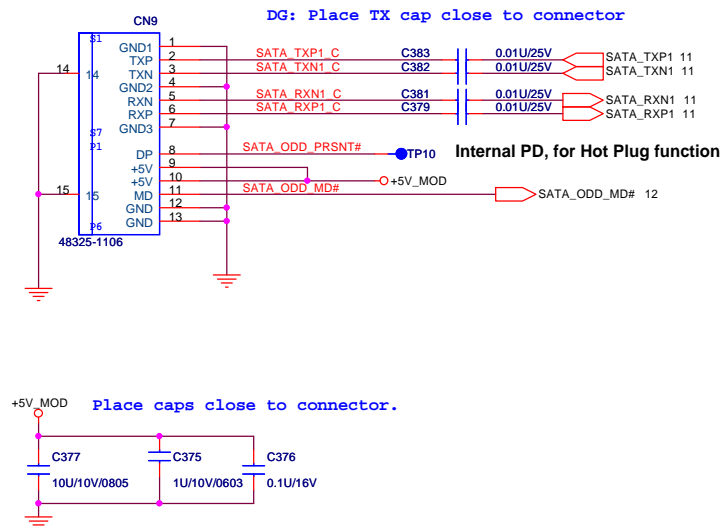


SATA Connector

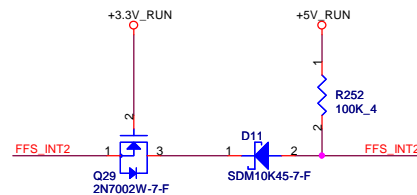
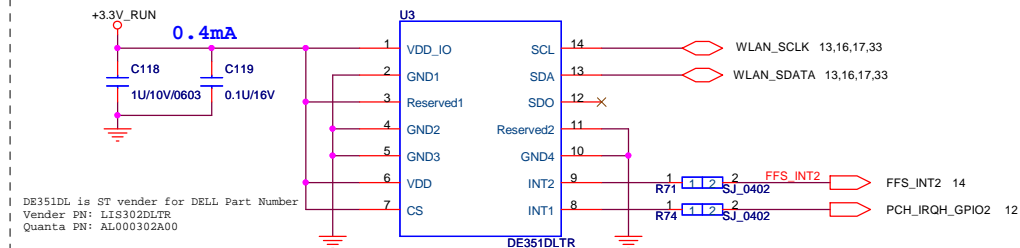
UM8



ODD Connector



3-axis Fall Sensor (HDD data protector)



3-axis Fall Sensor	VOSTOR	Inspiron
U3, Q29, D11 R71, R74, R252 C118, C119	POP	NC

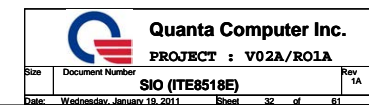


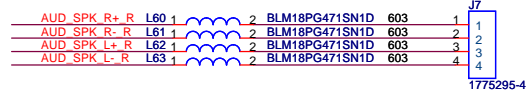
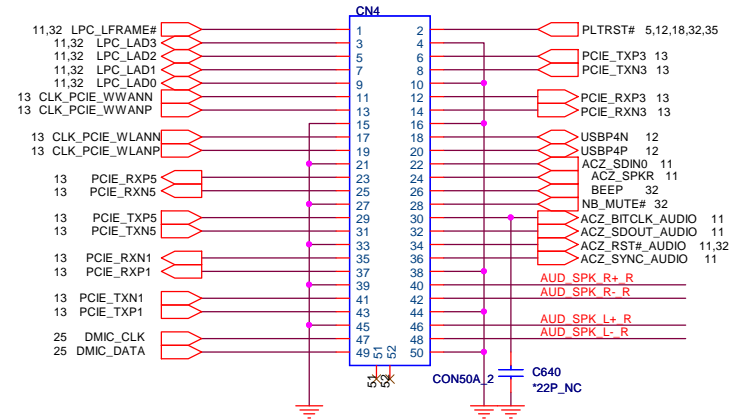
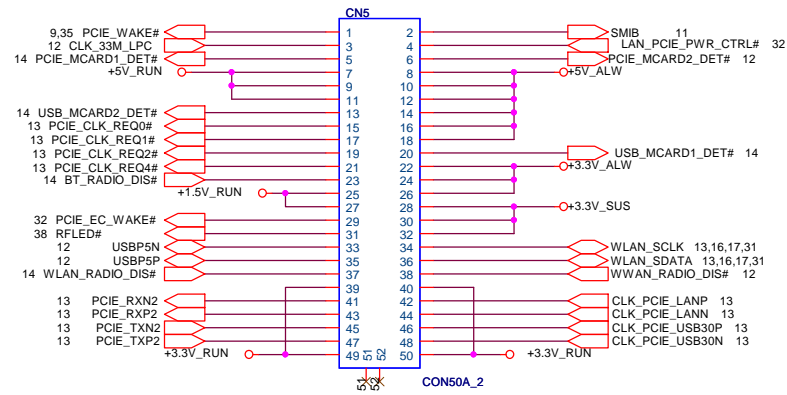
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PROJECT : V02A/RO1A

Size	Document Number	Rev
	SATA HDD/ODD	1A

Date: Wednesday, January 19, 2011 Sheet 31 of 61





Int. Stereo Speakers
5V / 4 Ohm / 2W

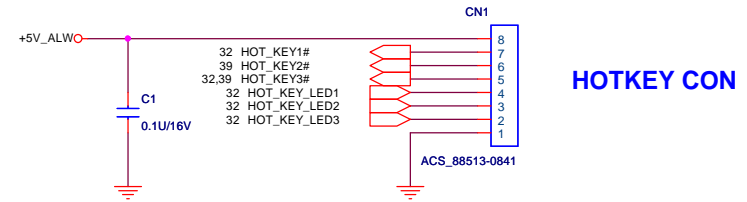


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PROJECT : V02A/R01A

SIO (ITE8518E)

Size	Document Number	Rev
		1A
Date:	Wednesday, January 19, 2011	Sheet 33 of 61



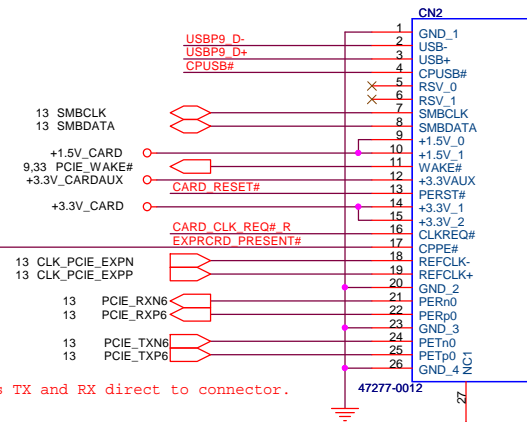
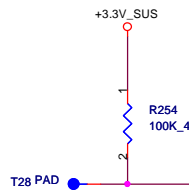
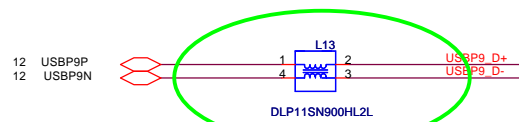
Quanta Computer Inc.

PROJECT : V02A/R01A

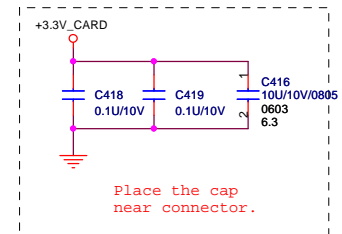
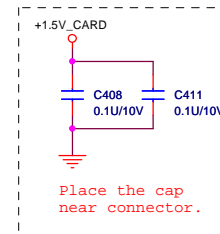
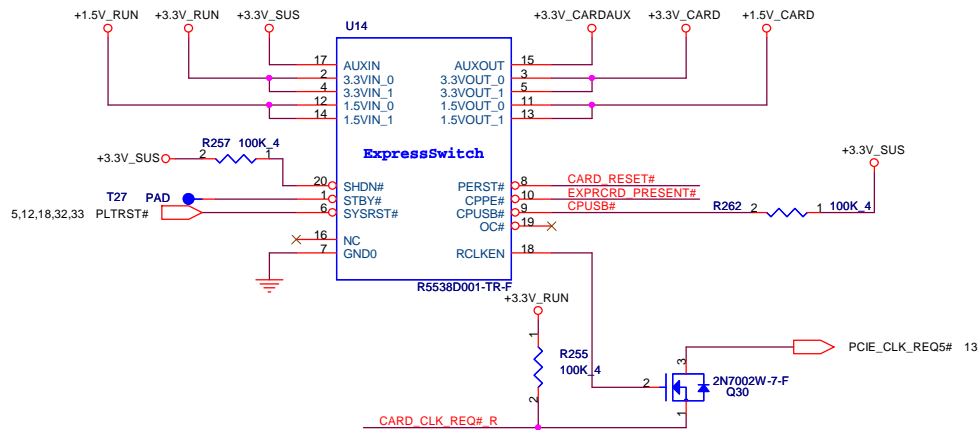
Size	Document Number	Rev
		1A

MINI-PCI (WLAN/WPAN)

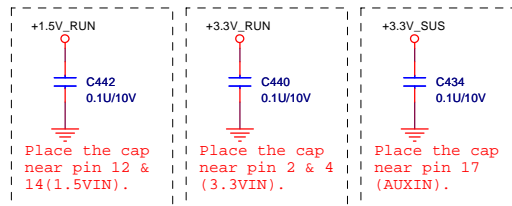
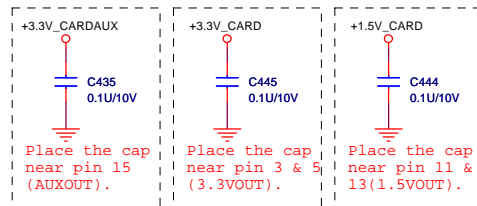
Date: Wednesday, January 19, 2011	Sheet 34 of 61
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+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



If close enough, could combine

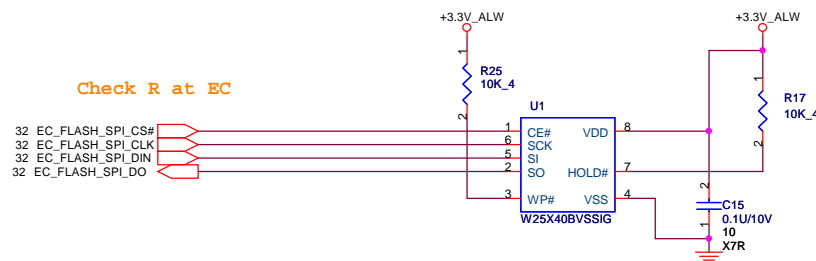


Quanta Computer Inc.

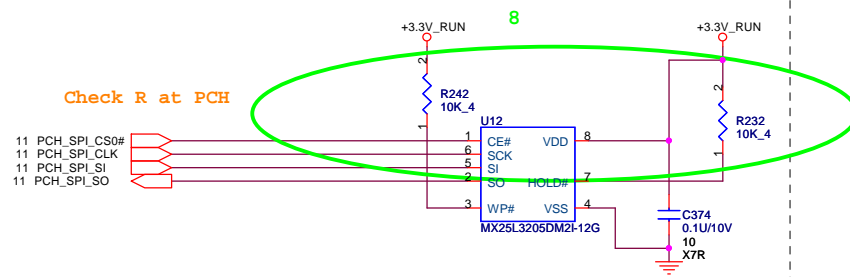
PROJECT : V02A/RO1A

Size	Document Number	Rev
	LAN (RTL8111EL)	1A
Date:	Wednesday, January 19, 2011	Sheet 35 of 61

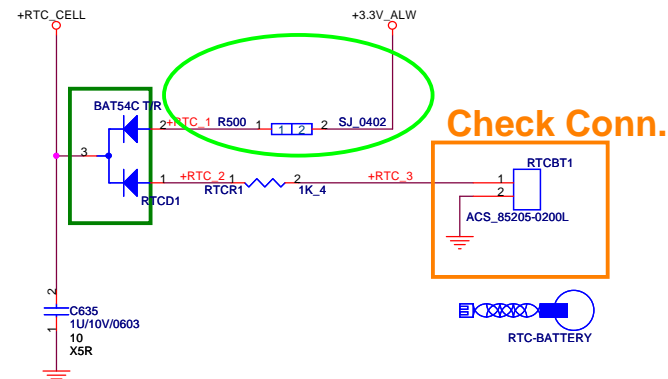
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC



Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA



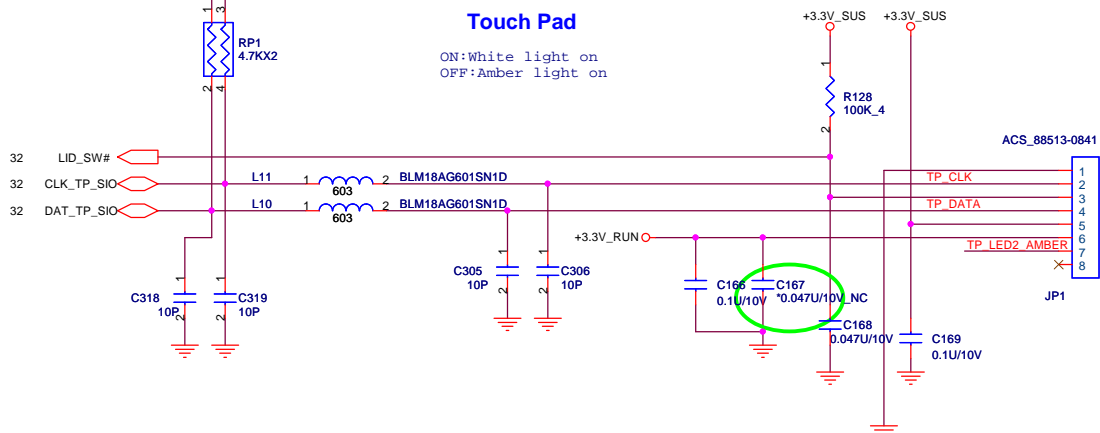
Quanta Computer Inc.

PROJECT : V02A/RO1A

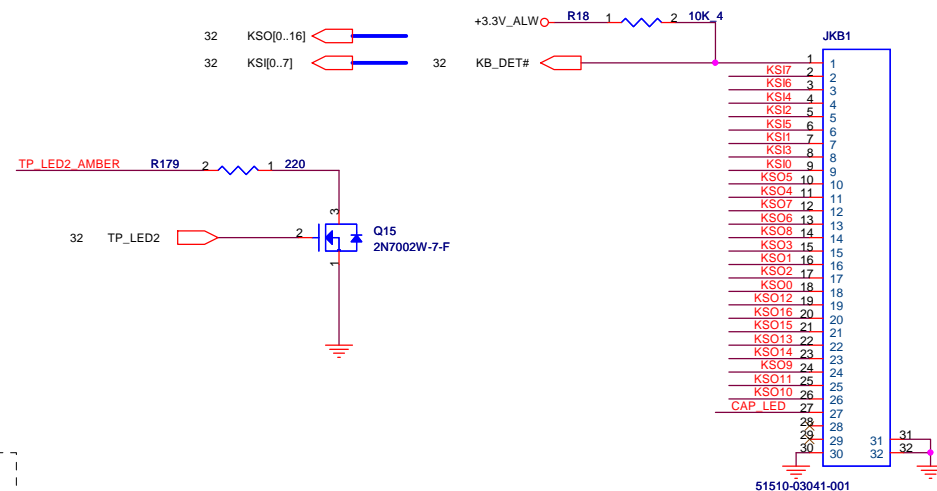
Size	Document Number	Rev
	FLASH / RTC	1A
Date:	Wednesday, January 19, 2011	Sheet 36 of 61

Touch Pad

ON:White light on
OFF:Amber light on

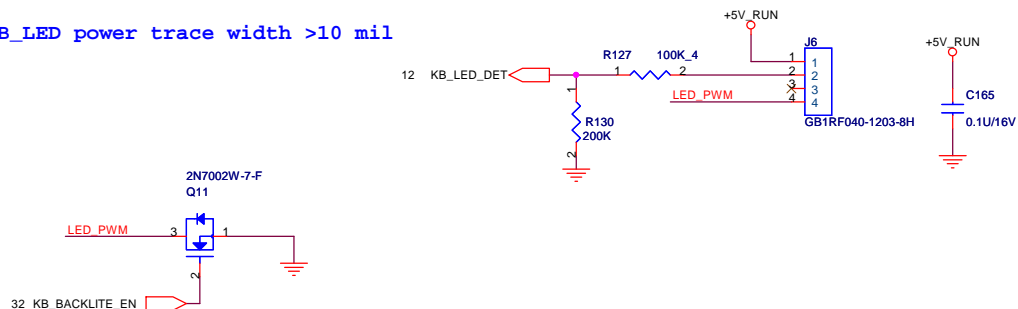


KEYBOARD CONNECTOR

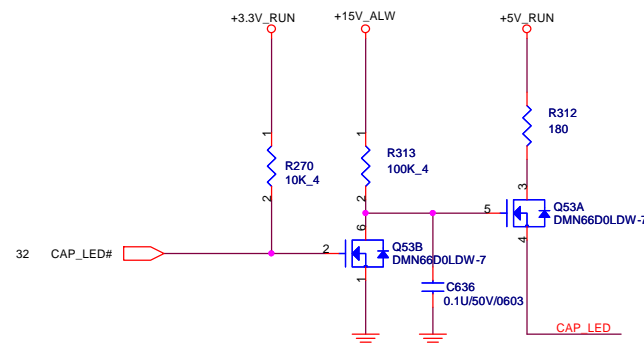
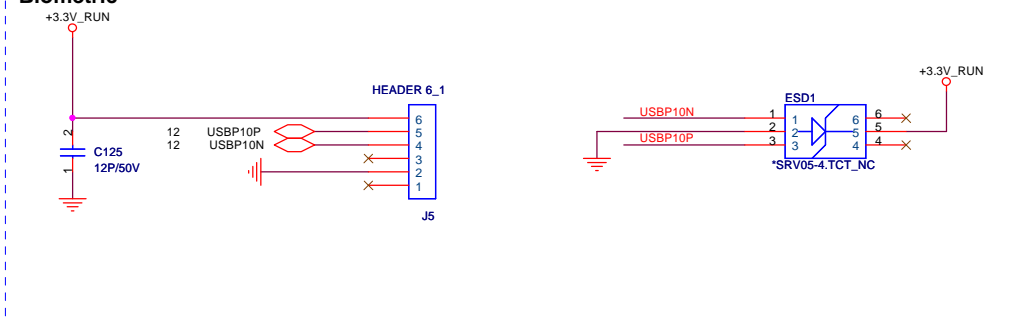


Key board illumination

+KB_LED power trace width >10 mil



Biometric

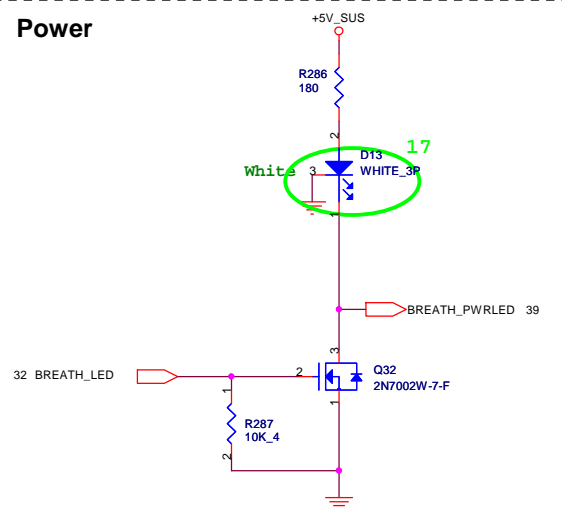


Quanta Computer Inc.

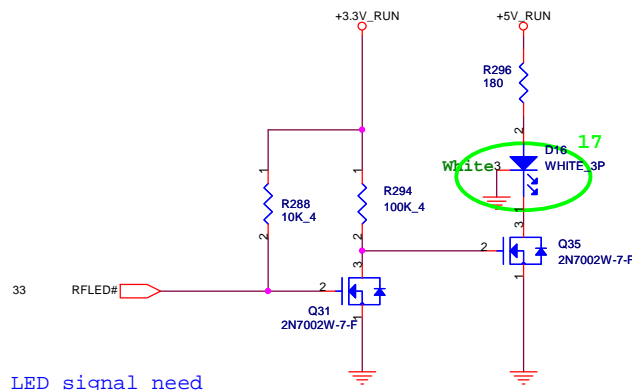
PROJECT : V02A/RO1A

Size	Document Number	Rev
	TP / KB	1A
Date:	Wednesday, January 19, 2011	Sheet 37 of 61

Power

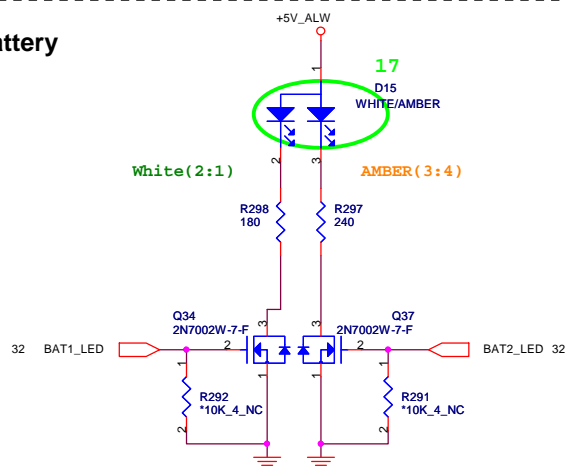


Bluetooth / WLAN on/off LED

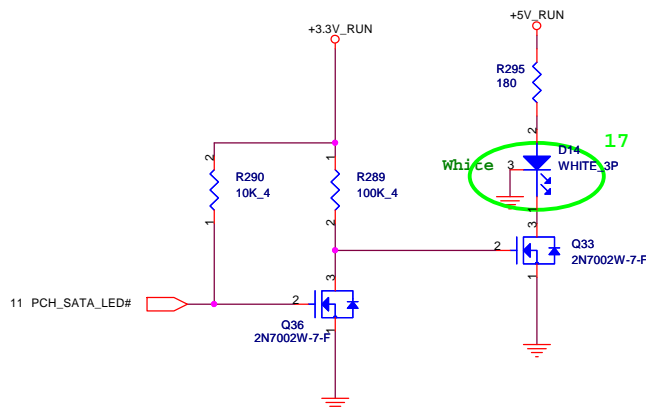


BT LED signal need

Battery



HDD activity LED.



VOSTOR	R286,R295,R296,R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286,R295,R296,R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

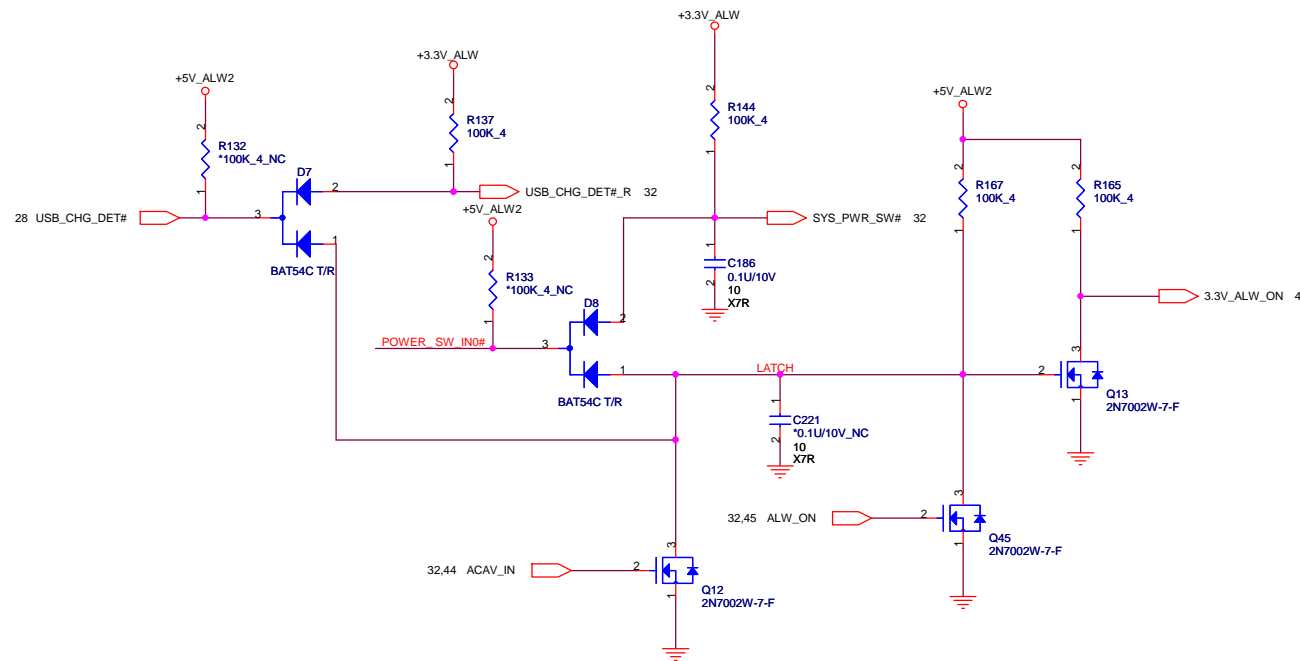


Quanta Computer Inc.

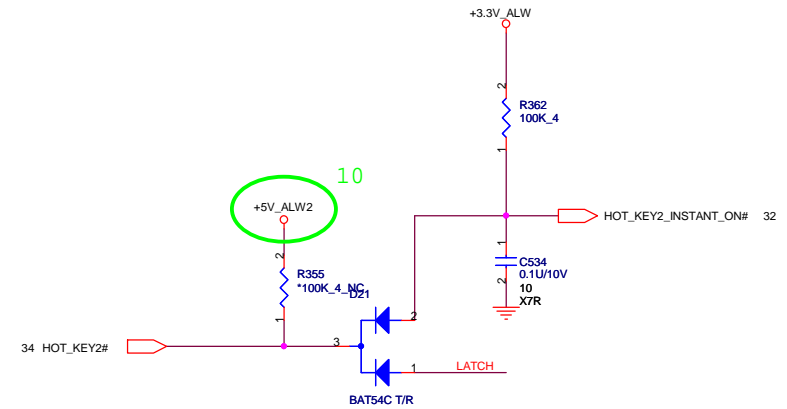
PROJECT : V02A/RO1A

Size	Document Number	Rev
	LED	1A
Date:	Wednesday, January 19, 2011	Sheet 38 of 61

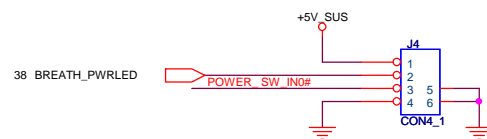
3VALW ON POWER LOGIC



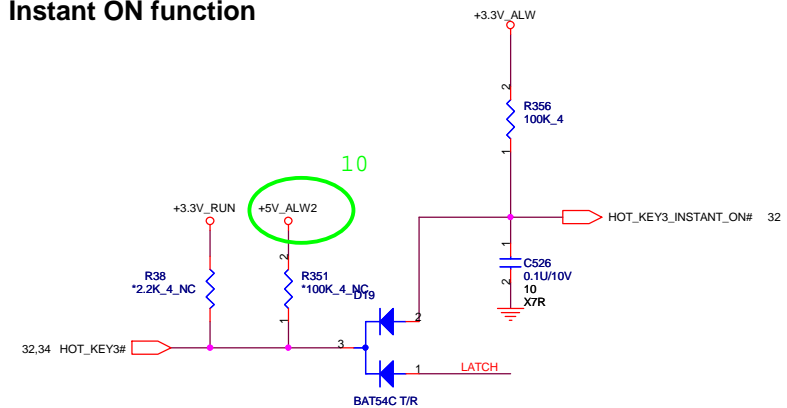
Vostro pop D19,C526,R356 depop R38,R39
Inspiron depop D19,C526,R356 pop R38,R39



PWR button board



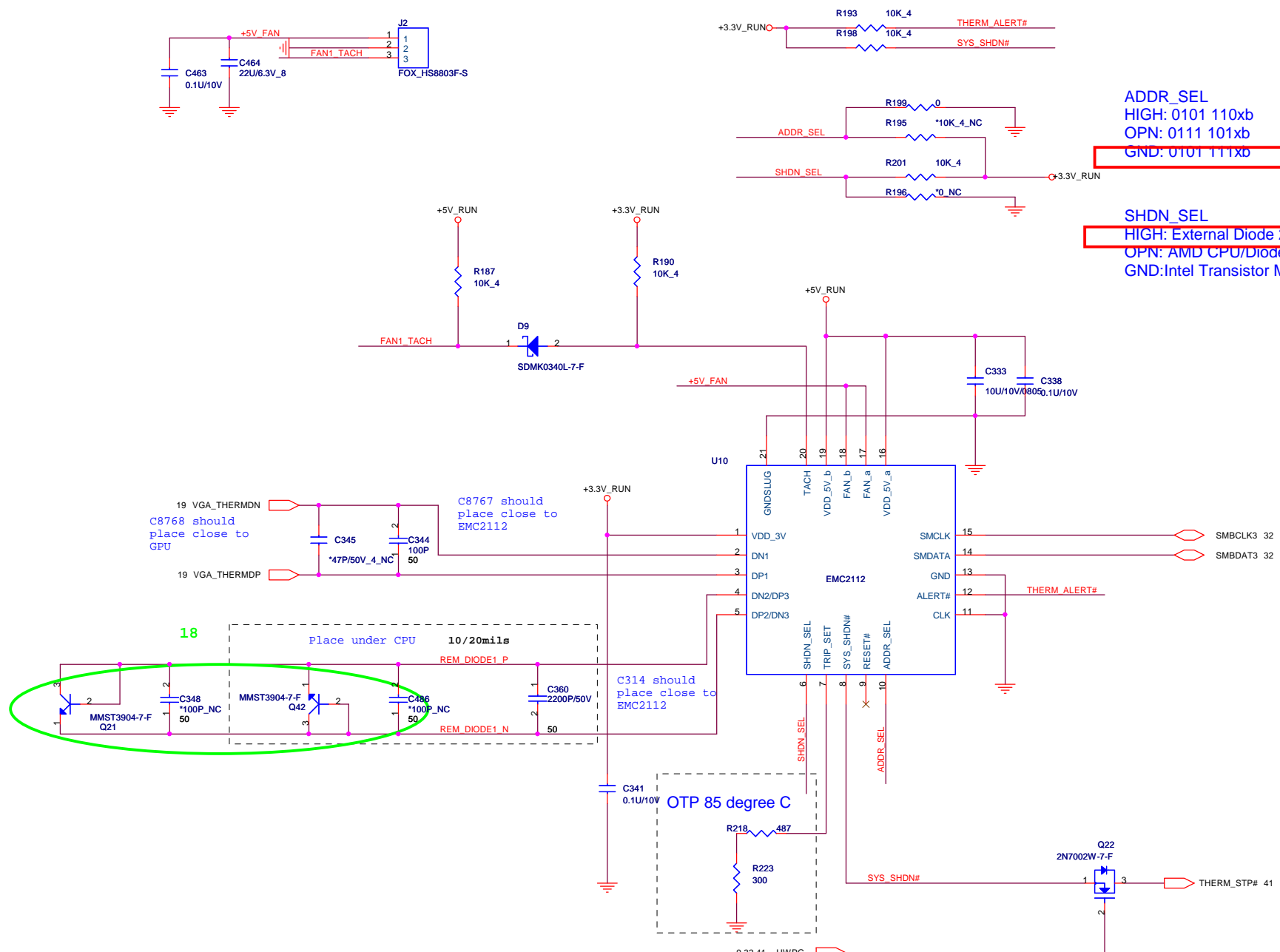
Instant ON function



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PROJECT : V02A/R01A

Size	Document Number	Rev
	PWR SW/LED	1A
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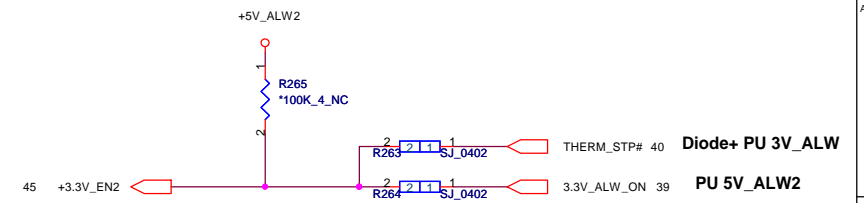
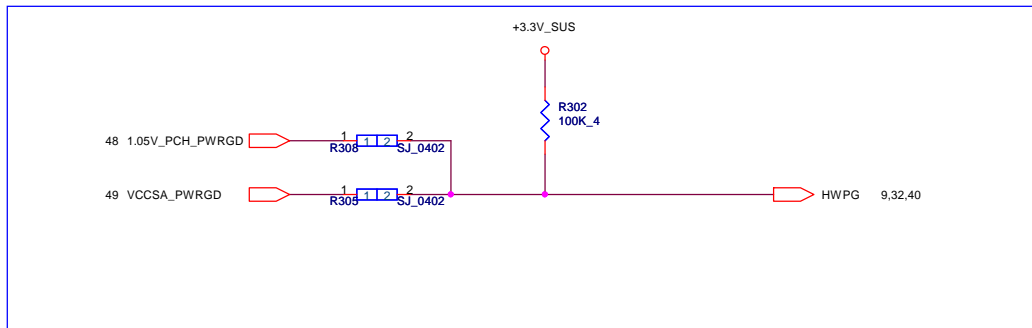
ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb

SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND: Intel Transistor Mode



Quanta Computer Inc.
PROJECT : V02A/RO1A

Size	Document Number	Rev
	FAN & THERMAL	1A
Date:	Wednesday, January 19, 2011	Sheet 40 of 61

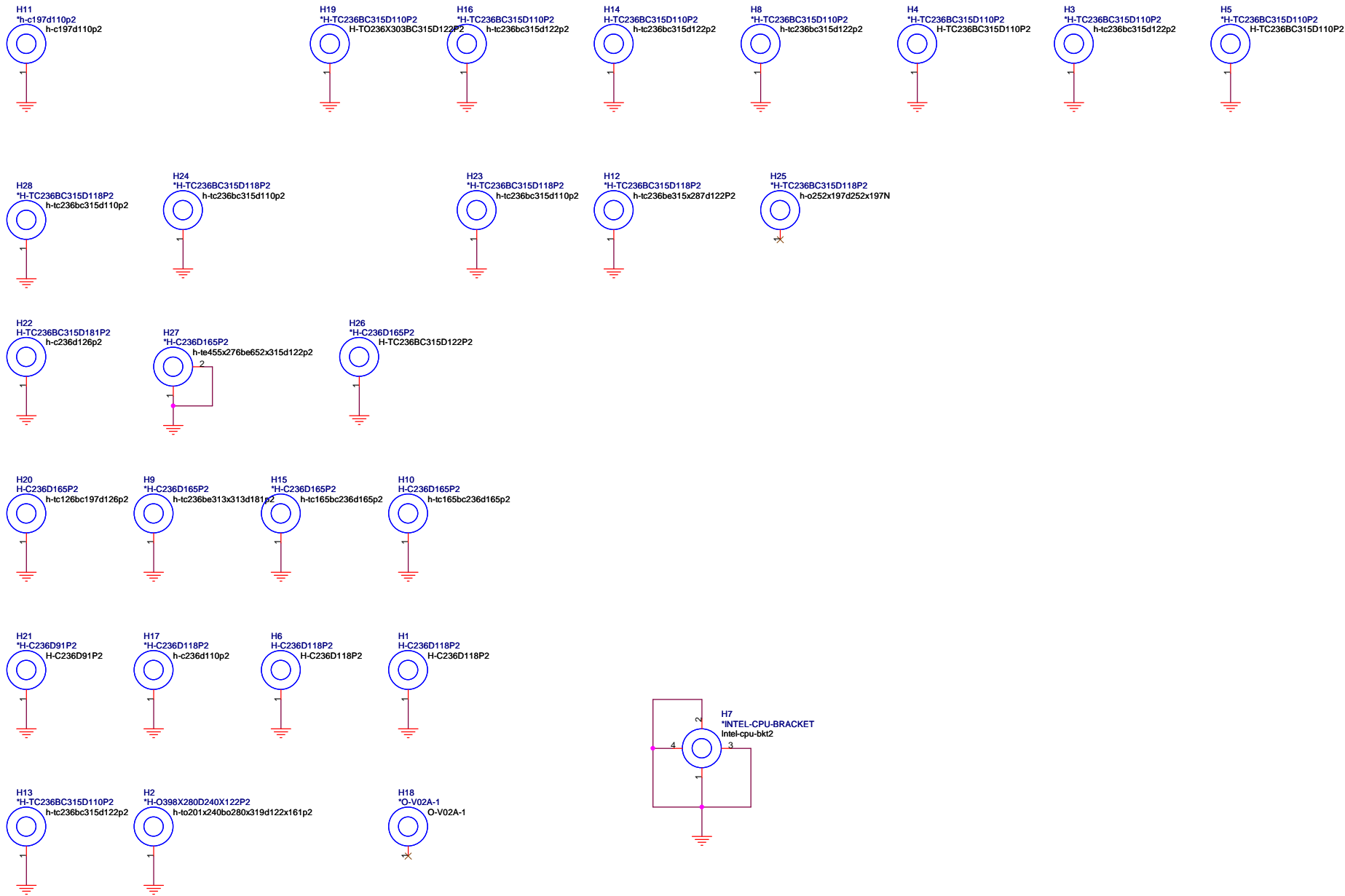


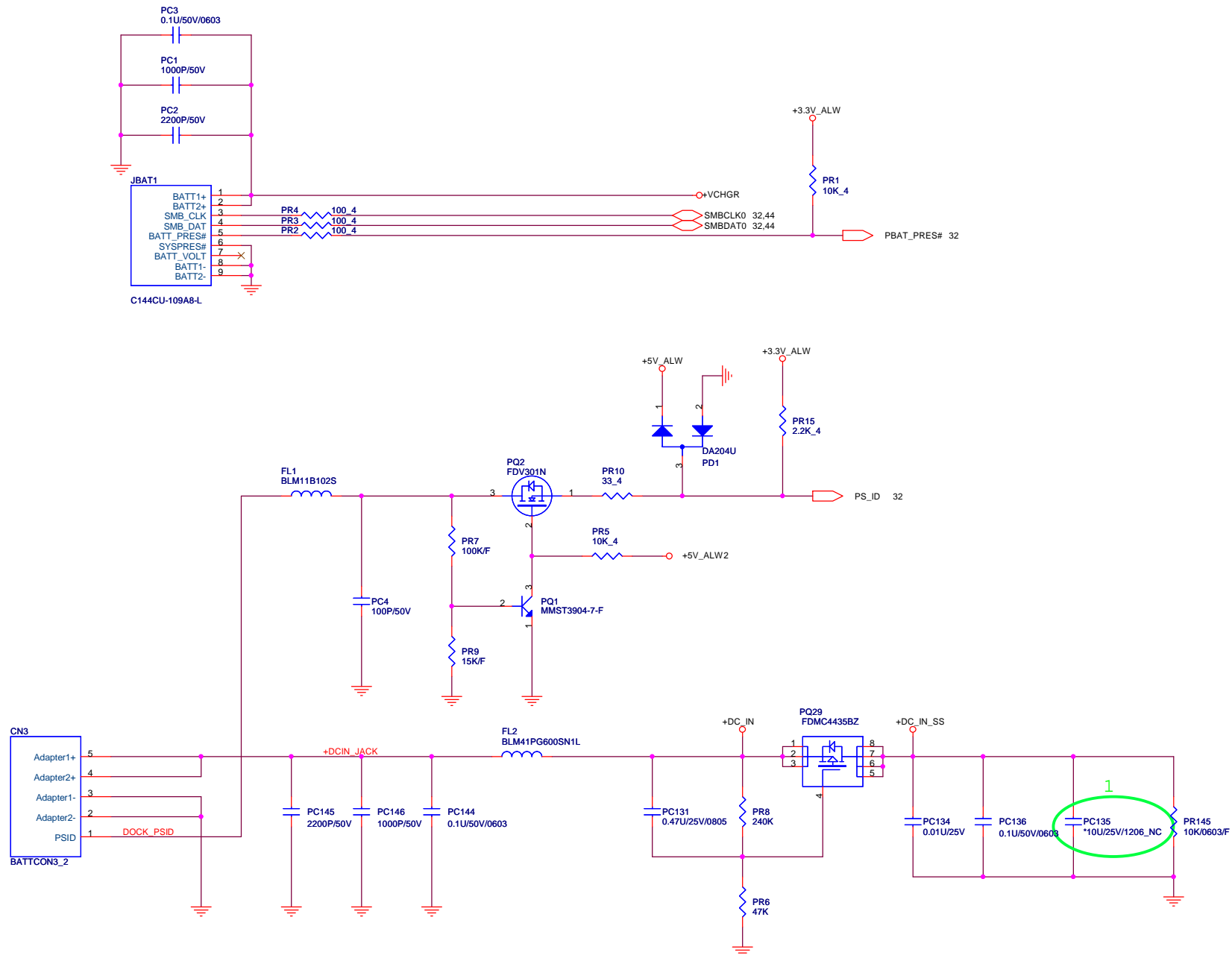
Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
		1A
Date:	Wednesday, January 19, 2011	Sheet 41 of 61

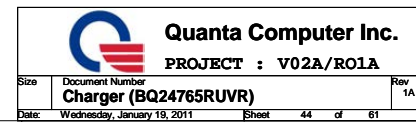
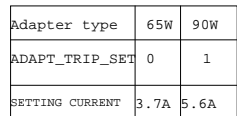
System Reset Circuit

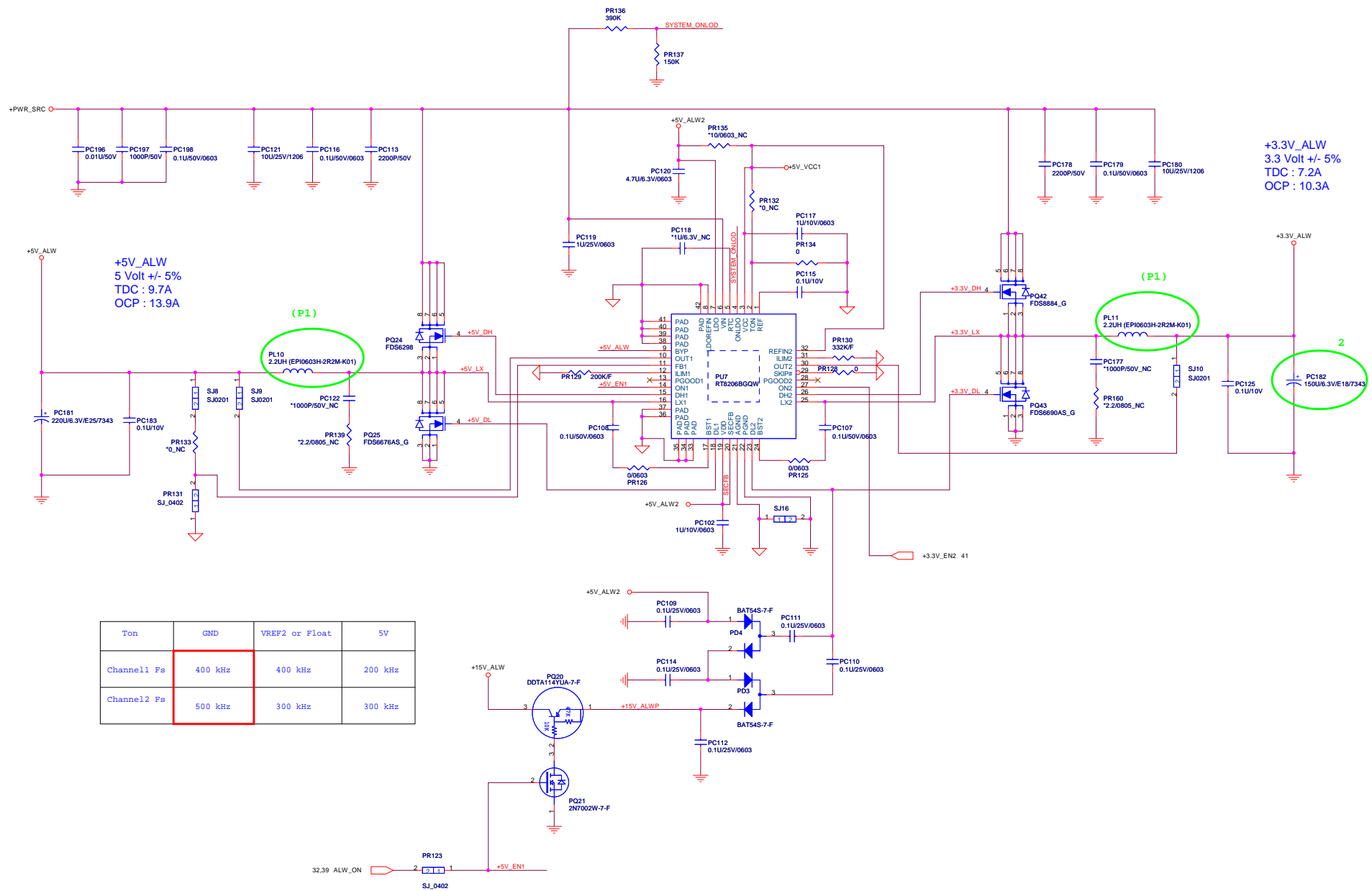


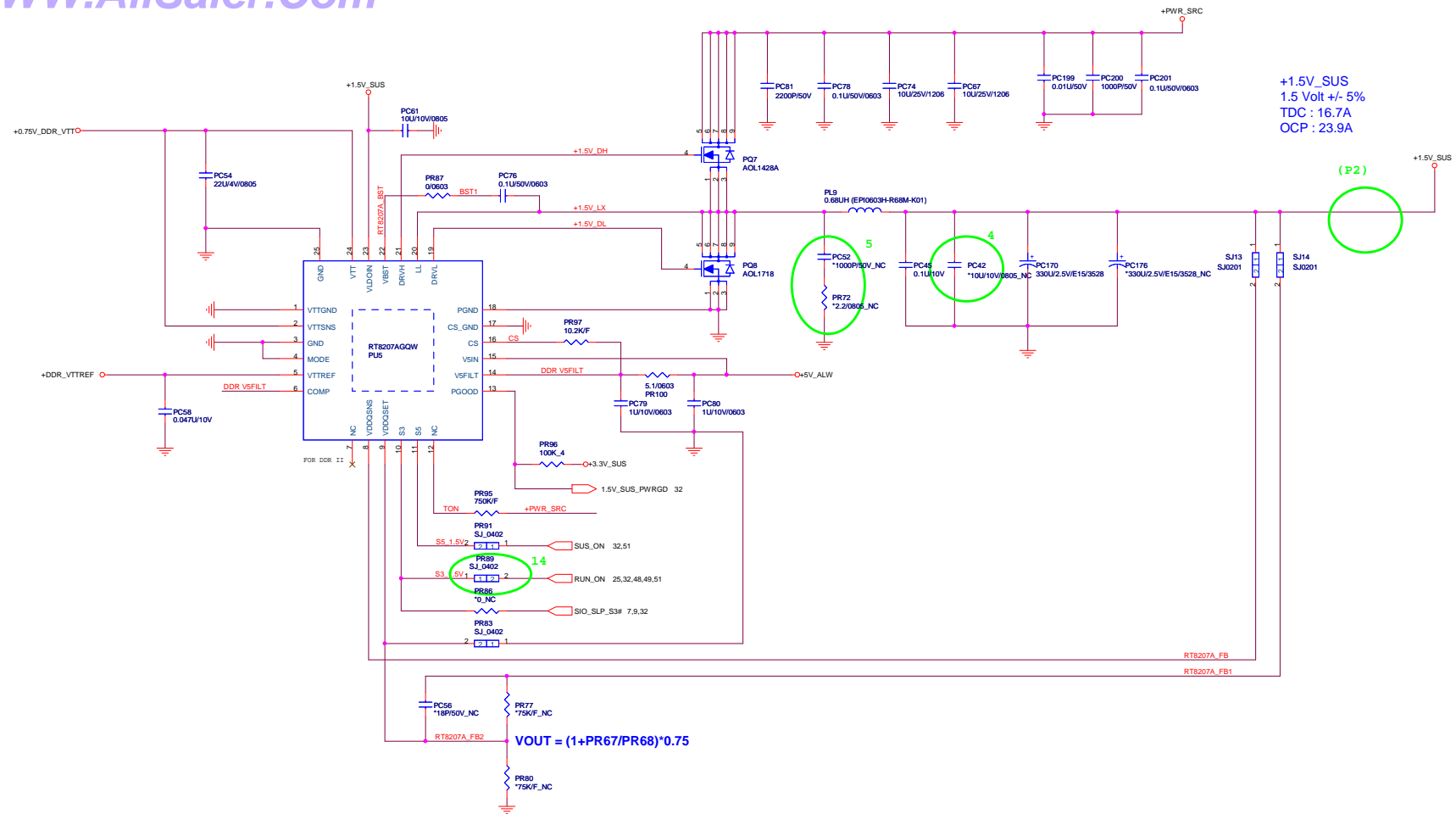


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PROJECT : V02A/RO1A

Size	Document Number	Rev
	DC IN / BATT	1A
Date:	Wednesday, January 19, 2011	Sheet 43 of 61







VDDQ and VIT discharge control

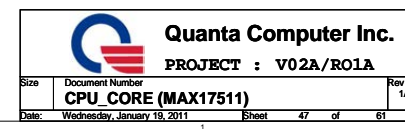
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

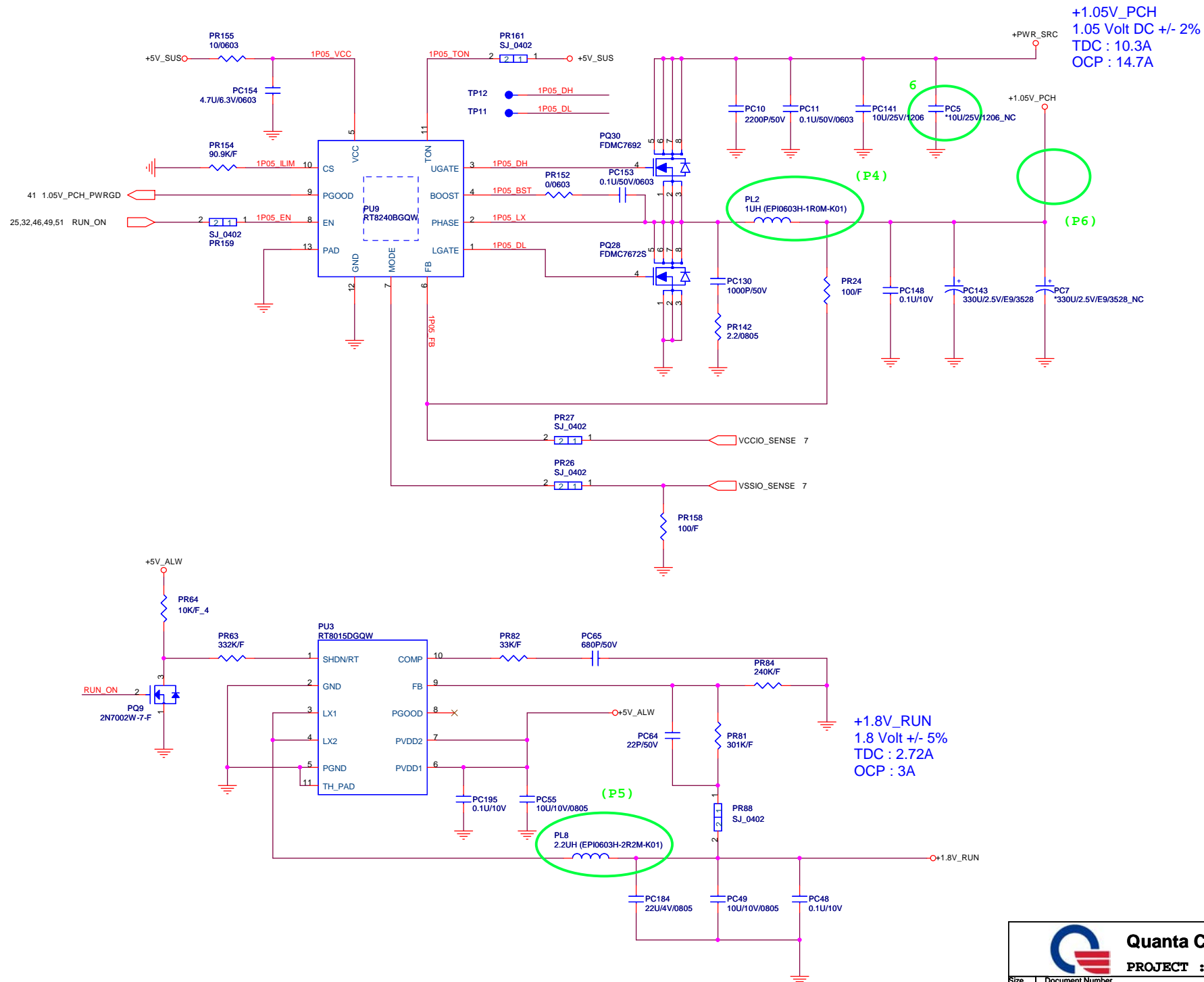
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VITREF and VIT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

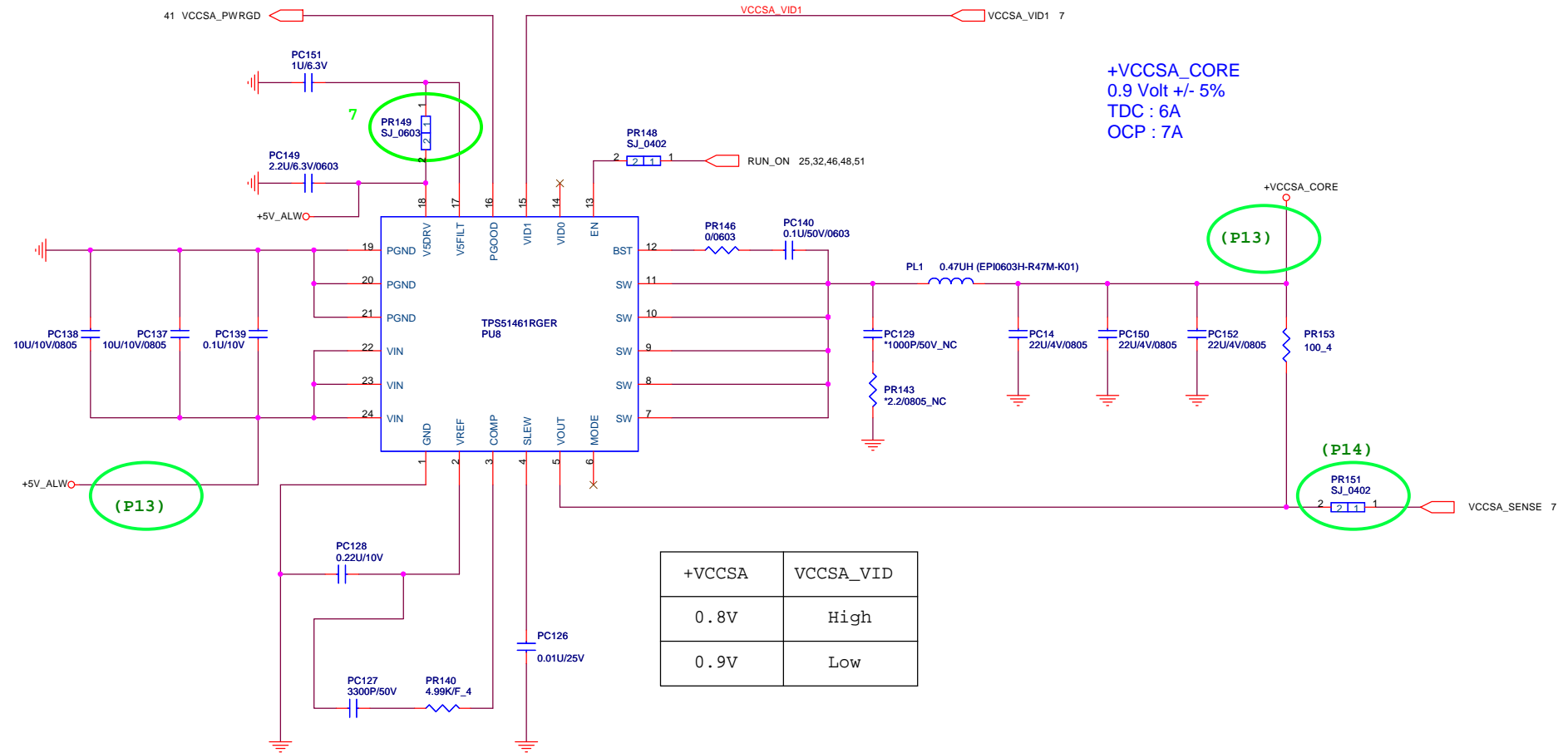
State	S3	S5	VDDQ	VITREF	VIT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



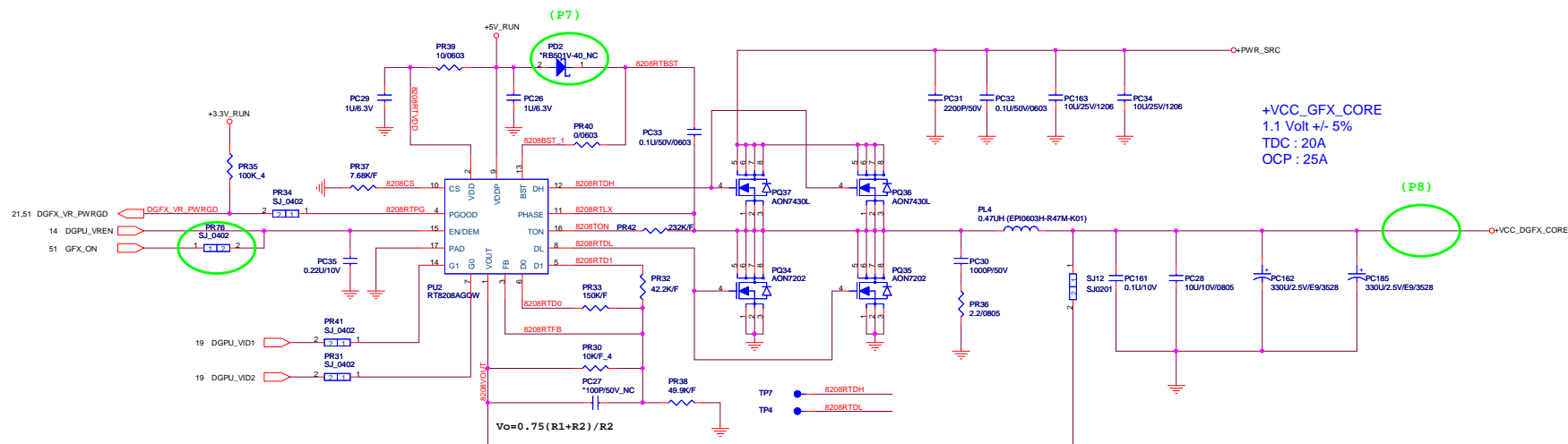


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PROJECT : V02A/RO1A

Size	Document Number	Rev
	+1.05V_PCH / VTT (TPS51218DSCR)	1A
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PROJECT : V02A/RO1A



Robson_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

Whistler_LP

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

Seymour_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K

